PROCESS SIMPLIFICATION FOR HIGH EFFICIENCY, SMALL AREA INTERDIGITATED BACK CONTACT SILICON SOLAR CELLS

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A baseline process for small area (4 cm^2) interdigitated back contact (IBC) silicon solar cells at imec is presented, based on n-type 156x156 mm^2 CZ silicon wafers. This process has been stabilised, and best obtained (calibrated) conversion efficiencies of 23.1% (average 22.8%) have been achieved. Recent developments have focused on process simplification, and are the subject of this report. The key findings include the benefits of introducing a wet oxidation step as the boron activation/emitter-passivation step (higher sheet resistance, lower J_0, and consequently higher efficiency). The surface cleaning routines have also been revised, resulting in slight increases in efficiency for simplified cleaning process (with consequent reduced process time/chemical consumption). Finally, results on contact definition by laser ablation are presented, showing a strong impact of the contact grid density on the BSF and emitter regions, on cell performance. The maximum achieved efficiency of 22.9% shows the potential for lithography replacement with an industrially viable patterning technique. These steps are driven by the goal of achieving a simplified and cost effective IBC process flow reaching high cell efficiencies.

Keywords: high efficiency solar cell, back contacted, wet oxidation, surface cleaning, laser ablation

1. INTRODUCTION

Interdigitated back contacted (IBC) solar cells have long been shown as high conversion efficiency solar cells, with values as high as 24.2% reported by Sunpower [1]. Such high efficiencies are enabled by the cell structure, with the absence of front side metal shading, which can then be optimised from optical and passivation perspectives. High bulk lifetime silicon and a low series resistance metal scheme also play a role in the efficiencies achieved. Other advantages include the easier module incorporation given both metal contacts are located on the rear of the cell. Given that both doped and contacted regions are located on the rear side, there are also additional challenges: more complicated processing than standard front side contacted solar cells, resulting from more patterning required to separate these doped regions (during fabrication and contacting), and sensitivity to contamination, given that both carrier types have to diffuse through the substrate bulk to be collected at the rear side.

At imec, a baseline high efficiency process has been developed on 2x2 cm^2 cells, initially using 4 inch FZ wafers [2], which has been extended to 125x125 mm^2 and more recently onto 156x156 mm^2 CZ n-Si [3]. This process uses extensive cleaning, high temperature oxidations, and lithography patterning to define the doped/contacted regions. In the past, efficiencies of 22.8% (on 125x125 mm^2), and 20.4% (on 156x156 mm^2) have been achieved with this process flow [3]. Although this process is not currently industrially viable, having such a stable and high efficiency baseline process enables comparisons between it and slightly modified processes, and examine their impact on the device performance. The focus of current research is to simplify the process flow, without compromising the final cell efficiency. Three key sections in this process flow are examined in this study, namely (A) emitter activation/passivation oxidation step, (B) cleaning step prior to high temperature processes, and (C) definition of the contacts through the passivation layers prior to metallisation. The motivation for this work is to report on recent updates to the process flow, their positive impact on the solar cell performance, thereby enabling the process to become more industrially-viable. It is shown that it is possible to reduce the time/thermal budget for the emitter oxidation step, and significantly reduce the sequence of wafer cleaning steps, without compromising the cell efficiency. First steps to replace lithography with laser ablation are presented, to define the contacted regions in the doped regions, which show promise for this technique in high efficiency IBC processing.

2. PROCESS FLOW

The baseline IBC flow at imec has previously been reported [3], but is again summarised here, where changes to the flow in this study are highlighted. Firstly, 156x156 mm^2 n-CZ wafers (ρ 1-4 Ω.cm) are thinned to 170 μm, cleaned and diffused with BBr_3. The emitter dopant activation/passivation is performed by thermal oxidation (see section 3.1 below). The back surface field (BSF) regions are defined by lithography; with the boron doped layer etched from BSF/front side, before cleaning BSF $POCl_3$ diffusion and thermal oxidation drive-in/passivation. At this point, the oxide on the front side is removed, the silicon surface is textured, and subsequent to cleaning, the front surface field (FSF) is diffused and oxidized, before an SiN_x anti-reflective coating is deposited. A cleaning step is foreseen before every diffusion and drive-in (see section 3.2). By another photolithography step and subsequent etching (see section 3.3), contacts are defined in the oxide layers protecting the emitter and BSF regions, before full wafer metallisation. The metal pattern is defined by another litho and etch sequence, before annealing, and finally

dicing into the 2x2 cm^2 solar cells reported in this work. Process and device monitor wafers are used for selected process steps, to gain an insight into the impact of each process step on the overall device performance.

3. RESULTS

3.1. Emitter activation/passivation

Activation of diffused dopant layers is critical to engineering the dopant profile of the layer, and the passivation thereof. Given that this region encompasses the majority of the rear side of an IBC solar cell, the significance of this step cannot be underplayed. Previously, a high temperature (1050°C) dry oxidation was performed for this purpose, yielding J_{0e} values in the region of 80 fA/cm^2 on 125x125 mm^2 CZ wafers [3]. In this study, a split in this oxidation step was considered, with either a dry or wet oxidation performed. The wet oxidation was performed at lower temperature than the 1050°C dry oxidation, as less bulk degradation due to oxygen precipitation is observed under such conditions [4]. The measured sheet resistance after oxidation is 83 Ω/sq for the dry oxidation, while after a wet oxidation, the sheet resistance increases to 97 Ω/sq. This results from a less deep boron profile after the wet oxidation step than the dry oxidation step. Consequently, by replacing the dry oxidation with a shorter wet oxidation step, the emitter saturation current density reduces from 51 to 24 fA/cm^2. It is noted that the value for dry oxidation (51 fA/cm^2 is higher than that reported above (81 fA/cm^2). This is explained by using silicon with higher bulk lifetime in the recent experiments than were used on 125x125 mm^2 wafers. When integrated at cell level, this change results in increased average and best cell efficiency, as shown in Table 1.

Table 1: Average and best results of illuminated IV of cells fabricated with dry and wet oxidation steps, measured on 2x2 cm^2 solar cells, using a calibrated reference cell. * denotes calibrated data from ISE CalLab, with designated illumination area measurement.

Oxide		J_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	η [%]
Dry	Average	41.20 ± 0.12	682 ± 4	76.6 ± 2.6	21.5 ± 0.7
	Best	41.25	690	79.8	22.7
Wet	Average	41.25 ± 0.31	691 ± 3	77.2 ± 2.9	22.0 ± 0.8
	Best	41.33*	689*	80.2*	22.8*

The averaged data (± sigma) are generated from 63 or 111 solar cells, for dry and wet oxidation respectively. This indicates a stable process, exhibiting higher best and average cell efficiency when a wet oxidation is performed. The change in V_{oc} is consistent with the reduction in J_{0e} for the emitter passivated with the wet oxide. Given the increased density of states at the Si/SiO_2 interface after wet oxidation [5], this finding is somewhat surprising. The high frequency capacitance-voltage response was measured at 1 kHz, and from these the interface state density profile has been extracted, using the method described by Berglund [6]. The CV plots are shown in Figure 1, and the inset shows the extracted density of states profiles, for wet and dry oxide layers. The difference between the wet and dry oxide layers is negligible, in terms of interface state density, and less so after forming gas annealing, performed to replicate the device process on the test samples.

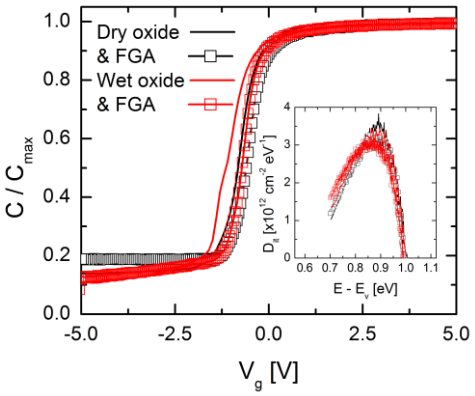

Figure 1. Capacitance voltage results measured at 1 kHz on $Si/SiO_2/Al$ samples. Results are presented for SiO_2 layers fabricated by wet and dry oxidation steps, both before and after a forming gas anneal step. The density of states profile as extracted from the CV data is shown in the index.

This plot clearly shows that the change in V_{oc} and J_{0e} after the wet oxidation step is not related to modifying the SiO_2 layer, or its interface with the silicon substrate. Also seen in table 1 is a slight increase in fill factor after the wet oxidation, which may also arise from a difference in dopant profiles after the oxidation steps examined. However, as the surface doping and contact resistance values were unchanged, this is unlikely to be the case. To summarise, the origin of the difference in V_{oc} and resultant efficiency measured in the solar cells results from a difference in boron doping profile, whereby the less deep profile after wet oxidation yields higher efficiencies.

3.2. Impact of cleaning step on solar cell performance

The presence of particulate, organic, and metallic impurities can have significant impact on surface and bulk lifetime [7]. This is a critical aspect for solar cells where the photo-carriers are generated on the front side, and collected on the rear side, as in the case for IBC cells. For this reason, in our baseline process, an extensive cleaning sequence optimised for high efficiency FZ-based silicon is performed prior to every high temperature process, a total of six process steps, as follows: (i) BBr_3 diffusion, (ii) oxidation, (iii) $POCl_3$ BSF diffusion, (iv) oxidation, (v) $POCl_3$ FSF diffusion, and (vi) oxidation. These six cleaning sequences are extensive, both in process-time and chemical-consumption. There is a clear advantage in replacing these sequences with abbreviated clean sequences. To this end, the cleaning processes prior to high temperature steps were varied, with three different combinations: the previously used extensive clean (A), an intermediate clean (B) and short clean (C). These steps were chosen to examine the impact of cleanings steps with various degrees of complexity. Minority carrier lifetime and J_0 values measured on samples which received the specified cleaning, before diffusion and/or oxidation steps, are

summarised in Figure 2. Clearly, no strong change in the saturation current density or minority carrier lifetime as a function of the cleaning steps, coupled with the high temperature processes which follow after, is observed. It is clear that the differences between the cleaning sequences indicate that there is no significant passivation/contamination modification revealed with the shorter cleaning steps, and such a simplification should not result in a compromise in solar cell efficiency.

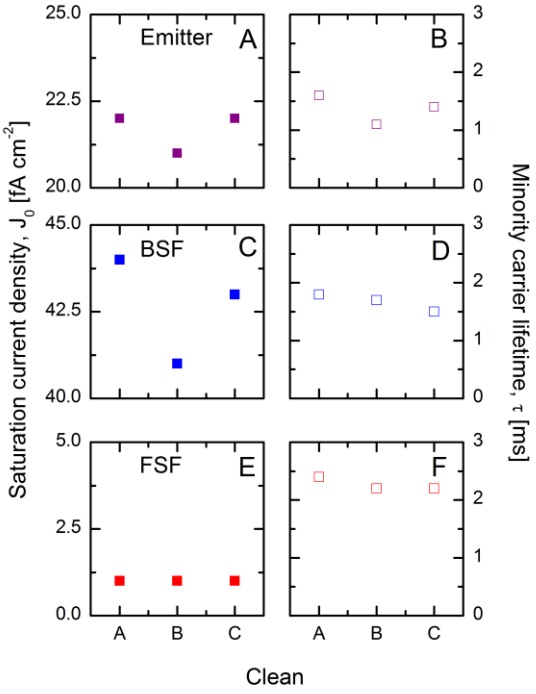

Figure 2: Measured recombination current density, J_0 (solid symbols) after (A) emitter, (C) BSF and (E) FSF diffusion (and subsequent drive-in), and effective minority carrier lifetime (open symbols), after (B) emitter, (D) BSF and (F) FSF drive-in processes, after the cleaning sequences employed in this work. Lifetime samples did not undergo the diffusion step.

From the J_0 and passivation test results, coupled with the solar cell results fabricated with the different cleaning sequences, shown in table 2, it is clear that all cleaning steps result in high-efficiency solar cells. The difference in the best-cell and average-cell efficiencies between the three cleaning sequences are within the error bars for the measurement, with a trend of increased efficiency with reduced cleaning complexity. These differences are related to changes in contact resistance observed. The conclusion drawn from this study is that for the CZ material used, reducing the complexity of the cleaning sequence does not come at a cost to cell efficiency, or distribution of cell results, thereby enabling a significant time and cost reduction.

Table 2. Average and best cell efficiencies measured for solar cells with different cleaning sequences prior to high temperature steps, measured on 2x2 cm^2 solar cells, using a calibrated reference cell. * denotes calibrated data from ISE CalLab, with designated illumination area measurement.

Clean		**J_{sc}**	**V_{oc}**	**FF**	**η**
		[mA/cm^2]	**[mV]**	**[%]**	**[%]**
A	Average	41.27 ± 0.23	689 ± 4	78.6 ± 1.6	22.4 ± 0.5
	Best	41.30	689	80.2	22.8
B	Average	41.30 ± 0.16	689 ± 3	79.3 ± 1.1	22.6 ± 0.8
	Best	41.61*	688*	80.7*	23.1*
C	Average	41.36 ± 0.14	690 ± 3	79.6 ± 0.9	22.8 ± 0.3
	Best	41.22*	688*	80.0*	22.7*

3.3 Electrically contacting the n^+ and p^+ doped regions

Contacting the rear junctions on IBC cells is performed by depositing the metal layer through a series of pre-defined vias in the SiO_2 passivation layers. This process involves selectively etching contact holes through the SiO_2 passivation layers that protect the emitter and BSF regions. For all results presented above, this patterning step is performed by a photolithographic masking step, and subsequent oxide etch, stopping at the silicon surface. In a bid to simplify the process, and evolve towards an industrially viable process, initial steps have been performed on opening contact holes by laser ablation, which has previously been shown as a viable tool for such processes on p-type FZ-Si [8].

In this case, a picosecond laser operating at 355 nm is used to ablate the oxide on both emitter and BSF regions, with fixed laser power in all cases, thereby ensuring the contact diameter is constant across all designs (albeit slightly larger for the BSF region than the emitter region). The contact fractions of the emitter and BSF regions were varied independently, by scanning the pitch of the contact holes ablated in the respective regions. The results are shown in Figure 3, where the measured V_{oc}, FF and efficiency are plotted as a function of BSF and emitter contact fraction, respectively. Also plotted in each case are the calculated cell parameters, derived using the 1 diode model (V_{oc}), where the J_0 value is weighted according to the contacted fraction of the doped layer. The fill factor is calculated using the measured resistive losses, and the efficiency is calculated as the product of J_{sc}, FF and V_{oc} values.

It is clear that the V_{oc} depends inversely on both emitter and BSF contact area, as shown in Figure 3A and 3B, with a stronger dependence in the case of the emitter than the BSF region. The impact of contact area on fill factor shows a strong dependence on the region, as shown in Figure 3C and 3D, whereby varying the emitter contact fraction reveals negligible variation in FF, whereas the FF increases strongly with BSF contact fraction. This trend is reflected in the response of the efficiency to contact area, where the overall trend indicates that the optimum efficiency is obtained for the highest BSF contact area (Figure 3E) and the lowest emitter contact area (Figure 3F). In all cases the calculated V_{oc}, FF and efficiency data correlates closely with the measured data. To summarise, strong impact of the contact fraction is observed, and

enables an optimum grid be defined which should result in further improvement in cell performance.

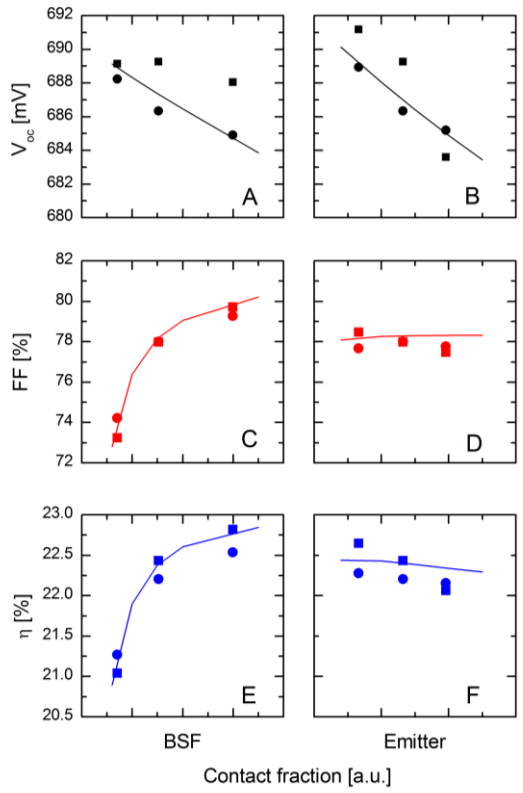

Figure 3: Impact of contact fraction of BSF (A, C, E) and emitter (B, D, F) doped regions, on small area IBC solar cell performance, namely V_{oc} (A, B), fill factor (C, D) and efficiency (E, F). Cells measured with calibrated reference, and shows that optimum efficiency is obtained for large BSF contact fraction, and low emitter contact fraction. Results were obtanied on 2x2 cm^2 solar cells, fabricated on 156x156 mm^2 wafers, measured with a calibrated reference cell.

The results measured after laser ablation in this experiment are benchmarked to those obtained when the contact holes are defined by lithography, and are summarised in Figure 4. In the plot, V_{oc}, FF and efficiency results are shown as a function of total contact area. In this case, the via density, either in the lithographic or ablation processes, defines the contact fraction to the cell. The contact fraction achieved by laser ablation is in the range achieved with lithography, but nonetheless the V_{oc} values are slightly lower, for a given contact fraction. The differences observed lie in the range 2-10 mV. The fill factor values are broadly in line for both lithography and laser processing (with the outliers explained by low BSF contact fraction, see Figure 3C), and the resultant efficiency results are slightly lower for the laser processed sample. The trends observed in Figure 3 for the laser ablated cells are repeated here for the litho patterned cells (i.e. V_{oc} reduces with contact fraction, FF and efficiency increase with contact fraction).

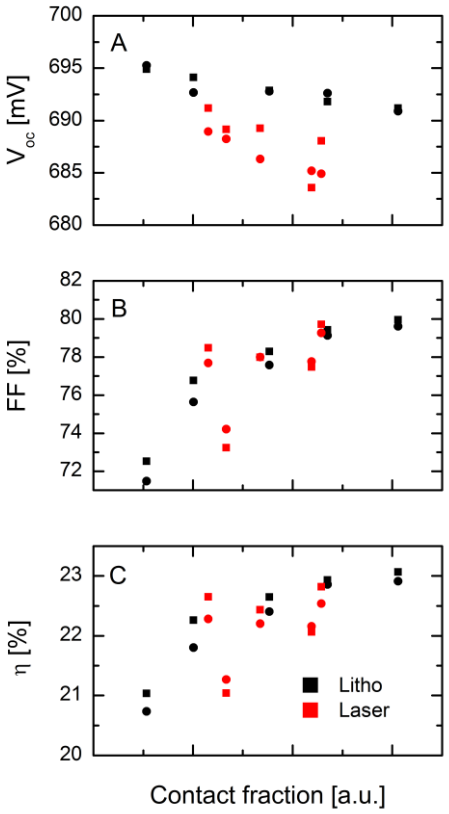

Figure 4. Plots of (A) V_{oc}, (B) FF, and (C) efficiency, plotted against contact fraction, for 2x2 cm^2 IBC solar cells, where the contacted region was defined by lithography (black symbols), or laser ablation (red symbols). Measured using a calibrated reference cell.

The best cell parameters obtained for both patterning methods are listed in Table 3, where the difference in V_{oc} and efficiency are 4 mV and 0.4%, respectively. It is noted that the contact fraction was not the same for these samples. The origin for this difference is somewhat related to this (given the impact of contact fraction, as shown above), and may also be related to laser induced damage of the silicon surface. Nonetheless, the results obtained in this work demonstrate the viability of laser ablation as a patterning technique to obtain high efficiency IBC solar cells. Further extension of this laser ablation process is the next foreseen evolution in the technology, where the BSF region would be defined by ablation in place of the lithography step currently performed.

Table 3: Best cell results of illuminated IV of cells fabricated with dry and wet oxidation steps, measured on 2x2 cm^2 solar cells, using a calibrated reference cell.

Contact definition	**J_{sc}**	**V_{oc}**	**FF**	**η**
	[mA/cm^2]	**[mV]**	**[%]**	**[%]**
Litho	41.73	692	80.7	23.3
Laser	41.75	688	79.7	22.9

4. CONCLUSIONS

Results are reported showing the developments and stabilisation of a baseline IBC process, where 2×2 cm^2 solar cells are fabricated on 156x156 mm^2 n-CZ wafers. Highest confirmed efficiencies of 23.1% have been achieved, and the key findings enable process simplification without compromising the cell efficiency. The latest changes include the benefits of a wet oxidation step after BBr_3 oxidation, as drive-in/emitter passivation. Due to the modified dopant profile due to this step, higher efficiencies are achieved. By simplifying the cleaning sequence employed before high temperature steps, improvements in the contact resistance and therefore efficiency are reported. Introductory results on defining the contacted regions by laser ablation show a strong dependence on the contact fraction of the emitter, and particularly of the BSF region. This enables efficiencies as high as 22.9% be achieved on laser ablated samples. coupled with incorporating replacements for the two other lithographic steps currently employed.

5. ACKNOWLEDGEMENT

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