DEVELOPMENT AND IMPLEMENTATION OF A PLATED AND SOLDERABLE METALLIZATION ON 15.6X15.6 CM² IBC CELLS

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ABSTRACT: IBC process development at imec has focused on upscaling from 2x2 cm² to full area 15.6x15.6 cm² cells, while making use of industrially viable processing techniques. First results were published recently, with a best cell efficiency of 21.3%, limited by a FF of 77.4% due to high series resistance. The process flow to obtain this result involved a 3 μm thick sputtered aluminium metal layer, which is not straight forward from an industrial perspective and not readily viable for module interconnection. We therefore developed a Cu-plated metallization for large area IBC cells. This metallization is the topic of this work. We developed and studied a suitable thin sputtered seed layer for the plating process, which serves as a barrier against Cu and which has good contact properties to Si. Sputtering of various materials could cause damage to the underlying passivation layer and Si, at cell level leading to lower V_{oc} and pFF. The damage caused by the different layers is investigated in detail and the developed process is implemented on 15.6x15.6 cm² IBC cells which yields efficiencies up to 21.9% over the full wafer area of 239 cm².

Keywords: Back Contact, Metallization, c-Si, n-type, Sputtering, Screen Printing, Silicon Solar Cell

1 INTRODUCTION

Interdigitated back contact (IBC) Si solar cells can be highly efficient. Record efficiencies up to 25.0% measured over an active area of 121 cm² have been demonstrated by SunPower, 25.6% on 143.7 cm² by Panasonic, and 22.9% on 239 cm² by Trina Solar [1,2,3]. These high efficiencies can be attributed to several advantages, including absence of front meal grid shading and reduced series resistance due to possibility of thick and wide metal contacts at the rear side.

At imec, a large area high efficiency IBC solar cell process has been developed by a platform based approach. Confirmed efficiencies > 23 % on small area 4 cm² cells on 15.6x15.6 cm² wafer were achieved using photolithography. A best cell efficiency of 22.7% on 4 cm² cells has been achieved with a photolitho-free IBC process using cost effective and industrially feasible patterning steps, and an sputtered metallization of 2 um thick aluminium [4]. Next, the cell area was scaled up to an IBC cell of 239 cm² covering the complete area of a 15.6x15.6 cm² wafer. The cell design for this large area IBC cells incorporates several rectangular unit cells connected in parallel [5]. This resulted in a best cell efficiency of 21.3% [6], limited by a fill factor value of 77.4% mainly due to high series resistance. Part of the solution to increase the FF would be to increase the metal thickness [4]. However increasing metal thickness by sputtering could lead to increased bowing and breaking of wafers. Additionally, sputtering thick AlSi by sputtering is neither commercially viable nor readily module capable [7]. Therefore there is a need to have a thick metal stack for IBC large area cells which is commercially feasible and compatible with module integration. A seed and Cu-plating process can tackle these challenges. This process requires a suitable seed layer stack that satisfies following requirements: good ohmic contact to both p^+ and n^+ doped silicon regions, high rear surface reflection, barrier for Cu diffusion into the Si and a suitable layer on top to enable subsequent plating. This thin stack could be easily deposited by sputtering owing to various advantages such as uniformity, maintaining stoichiometry and conformality [8]. However, sputtering of metal layers has been reported to cause damage to the underlying passivation layer and silicon substrate [9, 10, 11]. For sputtered AlSi layer this damage can be effectively recovered by forming gas annealing (FGA). However in some cases (metals such as NiV, NiCr) it has been shown that the damage cannot be fully recovered even after FGA [11].

In this study we report the development of a seed layer stack for Cu plating, its barrier properties, a detailed investigation of sputtering damage and its recovery by FGA. This seed layer stack and the subsequent Cu-plating process is then integrated in large area solar cells. In order to investigate applicability of inline Cu plating to thin wafers, Cu plating IBC cells was also performed on thin wafers of 130 μm thickness. All other standard cells and lifetime investigations were carried out on typical 170 μm thick wafers, unless explicitly stated otherwise.

2 PROCESS FLOW

The process flow used for the investigation of the sputtering damage is described below.

Firstly 15.6x15.6 cm² semi square n-type CZ silicon wafers undergo a saw damage removal etch step, are cleaned and either go for direct thermal oxidation (section 3.1) or undergo emitter (BBr_3) or BSF diffusion (section 3.2). The passivation/dopant activation is carried out by a thermal oxidation. This is followed by FGA and QSSPC measurements. Thereafter, on a part of wafers, contact areas are defined by laser ablation followed by various thin metallization stacks including two titanium based barriers, namely B1 and B2. These metal-silicon contact areas also allow investigation of possible Cu diffusion into silicon through the barrier. Thereafter the wafers receive an FGA followed by metal etch and photoluminescence imaging and QSSPC lifetime measurement. In order to analyse the surface defect density p and n-type polished and oxidized wafers were

used for capacitance voltage (CV) measurements. For these measurements the metallised areas were defined by photolithography after a blanket metal process and subsequent etch of the underlying seed layer.

3 RESULTS AND DISCUSSION

3.1 Studies on passivated wafers without BBr_3 or $POCl_3$ diffusion.

It is observed from Fig. 1 that samples with laser ablation show significantly lower lifetimes than samples without ablated surfaces, as in the laser openings obviously no passivation is present. It is also seen that samples with AlSi/B1 (and B2) display lower lifetimes ($\leq$ 1 ms) than those with AlSi only (>1.5 ms). It shows higher damage on samples with either barrier. It is noted that additional damage caused by deposition of the barrier is not associated with sputtering power as sputtering power used for barrier layers was significantly lower than for AlSi. Next, the samples with AlSi/B1/Cu and AlSi/B2/Cu display similar lifetimes as respective samples (AlSi/B1 or B2) without Cu, indicating that the Cu deposition and the FGA at 400 °C do not lead to Cu diffusion through the barrier layers, or that such a Cu diffusion has no further negative effect on the lifetime. However AlSi/B1/Cu showed slightly lower lifetimes in low injection regime (not shown) than AlSi/B2/Cu. Therefore barrier B2 was chosen for further investigations on samples with emitter/BSF diffusion (see section 3.2). Surprisingly non-ablated samples with AlSi/Cu show higher lifetime ($\geq$ 2ms) than corresponding samples with AlSi only. This shows Cu does not cause any significant sputtering damage and possibly results is enhancing lifetime by effect similar to the well-known Alneal effect [12].
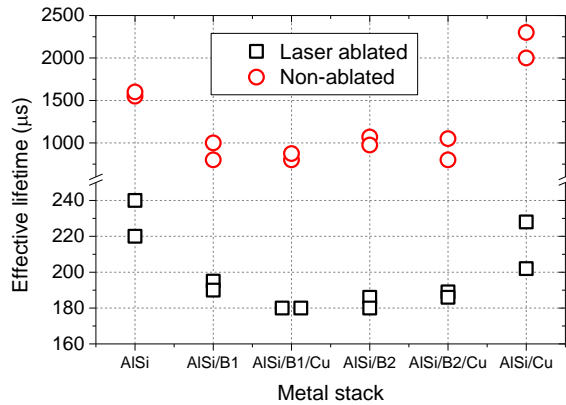

Figure 1: Final effective lifetimes (at injection level of 1e15 cm^{-3}) of oxidised samples after sputtering and etching different metal stacks.

However, this does not imply that no barrier layer would be required as the laser ablated AlSi/Cu samples display lower lifetimes than samples with only AlSi, which could be indicating Cu diffusion in the laser ablated regions. Various phases of Cu and Al are possible after sintering at 400 °C emphasizing the need of a barrier layer to prevent diffusion of Cu.

Capacitance–voltage profiling (CV) measurements carried on p and n type polished and thermally oxidized

silicon wafers are shown in Fig 2. Immediately after the seed layer sputter step, a large shoulder is present in the CV curves in the region between accumulation and depletion for both n-Si and p-Si substrates, consistent with presence of high densities of silicon dangling bond defects at the Si/SiO$_2$ interface, at energy levels between the valence band edge and midgap (on p-Si), and from midgap to the conduction band minimum (n-Si). These features are removed by forming gas annealing, indicating the successful passivation of the interface defects. Negligible hysteresis indicates low densities of traps/defects in the SiO$_2$ layer, after FGA for all samples with AlSi, AlSi/B2 and AlSi/B2/Cu. It has been reported [13] that sputtering introduces damage near the interface and these defects move deeper into the substrate at temperatures above 275 °C. These defects were shown to be present up to a depth of 0.5 μm. This results in important conclusion that the difference in effective lifetimes on samples with and without barrier layer are not related to any remaining surface damage but could be related to the shallow damage below the Si/SiO$_2$ interface.
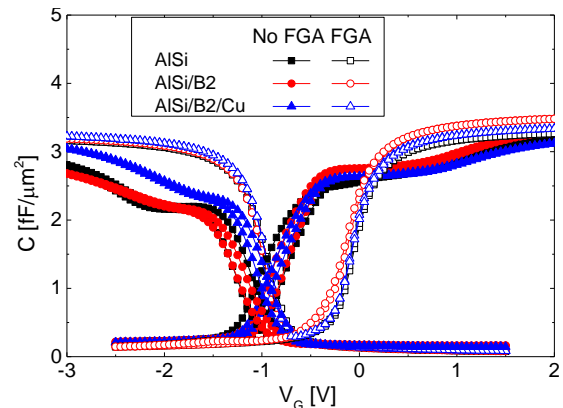

Figure 2: CV measurements on thermally oxidised p and n-type samples.

3.2 Studies on passivated wafers with BBr_3 or $POCl_3$ diffusion.

In order to understand the effect of sputtering damage on open circuit voltage and pseudo fill factor of IBC cells, samples with symmetrical emitter (BBr_3) and BSF ($POCl_3$) doping were prepared. These samples were sputtered with AlSi, AlSi/B2 and AlSi/B2/Cu layers. Lifetime and emitter saturation current (J_{0e}) values measured on these samples with AlSi and AlSi/B2/Cu after FGA (and metal etch) are shown in Fig 3. Firstly, it is observed that there is a very small difference in lifetimes between laser ablated and non-ablated samples for these diffused wafers (contrary to samples without and with doping shown in Fig 1). This can be attributed to the field effect passivation from the diffused regions masking the surface passivation damage caused by laser ablation. Secondly, for BSF diffused samples no measurable difference in lifetime or J_{0e} was observed between AlSi and AlSi/B2/Cu. Although the samples with emitter diffusion show slightly better lifetimes for samples with AlSi/B2/Cu than corresponding samples with AlSi, it was found this is related to the difference between effective lifetimes or the wafers measured before metal sputtering rather than to the sputtered layers itself.

These results are also in contrast to the results shown in Fig 1, on non-diffused samples. It was concluded from these studies (as well as from CV) that additional sputtering damage caused by barrier layer below the surface is possibly situated in the (highly) doped region of emitter and BSF diffusion. This is also in line with the above mentioned fact that the doped regions could screen the surface defects. Therefore if this sputtering damage exists, the measurement of J_{0e} and effective lifetime are not sensitive enough to measure any effect.
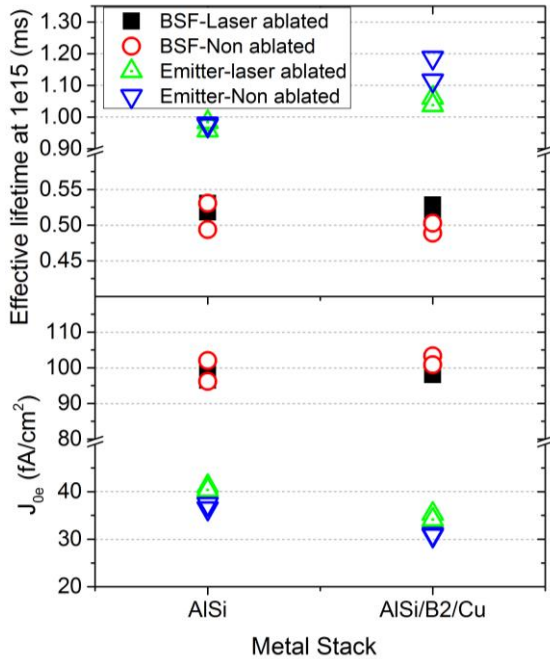

Figure 3: Effective lifetime (at injection level of 1e15 cm^{-3}) and Joe for emitter and BSF diffused samples.

4 CU PLATING PROCESS IMPLEMENTATION ON IBC CELLS

The process developed previously [4,6] is followed until opening the contact areas by laser ablation. Metallization is carried out by PVD AlSi/B2/Cu blanket deposition. Emitter and BSF metallised regions are defined by screen printing a resist followed by Cu plating on non-masked regions. It is followed by resist strip and metal seed etch. During the metal seed etch, the Cu acts as a mask so the seed layer is only etched in the regions without Cu, which are the regions were the resist was printed. Thereafter FGA and characterisation were performed.

4.1 Results of 1st batch of Cu plated cells

Results obtained on 1st batch of IBC cells with Cu plated metallisation are listed in Table I. It is observed that cells with AlSi and Cu plating based metallization display a similar open circuit voltage (V_{oc}). This confirms that sputtering damage caused by the additional barrier layer is effectively recovered. Very high pseudo fill factors are observed for Cu plated samples indicating absence of shunts in metallization and affirm that developed seed layer (barrier) is effective against Cu

diffusion [14] and the potential for such a metallisation scheme. However, low FF in spite of Cu metallization with higher thickness was noted. This is partially related to non-uniform local contact resistance, consistent with electroluminescence (EL) images shown in Fig 4 (a), similar to the EL features described in literature [15].

Table I: IV results on 239 cm^2 area IBC cells for the 1st batch.

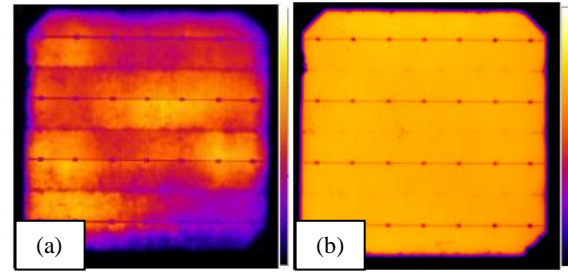| Metal	J_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	Eta [%]	pFF [%]
Cu plated	40.45	688	73.8	20.5	83.8
AlSi PVD	40.80	686	77.1	21.6	83.8

Figure 4: Electroluminescence images of typical Cu plated IBC cells (a) from 1st batch with non-optimised surface pre-treatment (b) from 2nd batch with optimised surface pre-treatment.

It has been reported [16], that the contact resistance of n$^+$ diffused (BSF) regions to AlSi depends very strongly on the sintering temp along with pre-sputtering surface cleaning. The contact resistance could decrease by two orders of magnitude depending on the effectiveness of the surface clean and the exact sintering temperature. Therefore a 2nd batch of cells were prepared with improved surface preparation and with higher sintering temperatures of 450 ˚C during FGA as compared to 400 ˚C FGA for the first batch of cells.

4.2 Results of 2nd batch of Cu plated cells: Improved surface pre-treatment and FGA

The native surface oxide in the contact area was removed by means of longer (30 sec) dip in dilute HF as compared to 10 sec dip previously used. The results obtained for both FGA sintering temperatures of 400 ˚C and 450 ˚C with longer HF dip are listed below in Table II.

As seen from Table II, cells with both 400 ˚C and 450 ˚C FGA display significantly higher fill factors than cells from the 1st batch listed in Table I. A typical EL image of the cells obtained in the 2nd batch is shown in Fig 4 (b). Clearly, the local non-uniformities seen in Fig 4 (a) are not visible anymore in this case. Thus, the issue with contact resistance is resolved by longer HF before metallization. Good control of surface (HF dip) before metallization avoids problems with contact resistance. Contact sintering in FGA at 400˚C or 450˚C does not

show any significant difference.

Table II: Average (of results form 5 cells) IV results on 239 cm^2 area IBC cells for the 2nd batch.

Contact sintering	Size [cm^2]	J_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	Eta [%]	pFF [%]
FGA 400˚C	239.1	40.32 ±0.10	680 ±1	78.3 ±0.2	21.5 ±0.1	82.7 ±0.1
FGA 450˚C	239.1	40.21 ±0.14	679 ±2	78.4 ±0.3	21.4 ±0.2	82.8 ±0.1

Best results obtained with Al-PVD and Cu plated metallisation are listed in Table III. IBC cells with Cu-plated metallization display higher fill factor as compared to 3-μm AlSi PVD metallization. This is maily due to the lower line resistance of the Cu metallization. Best efficiency of 21.9 % measured over full area of 239.1 cm^2 is achieved with Cu plated IBC cells.

Table III: Best IV results on 239 cm^2 area IBC cells with AlSi and Cu plated metallisation.

Metal	Size [cm^2]	J_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	Eta [%]	pFF [%]
Cu plated	239.1	40.64	682	79.0	21.9	83.0
AlSi PVD	239.1	40.80	686	77.1	21.6	83.8

4.3 Cu plated IBC cells on 130 μm wafers.

As mentioned earlier, in order to investigate applicability of inline Cu plating to thin wafers, Cu plated IBC cells were also prepared on 130 μm silicon wafers. The results on thin wafers are presented below in Table IV.

Inline Cu plating for thin 130 μm IBC cells was carried out by Meco Equipment Engineers.

Table IV: Average and best cell IV results on 239 cm^2 area IBC cells with Cu plated metallisation and 130-μm thick wafers.

	Size [cm^2]	J_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	Eta [%]
Average (8 cells)	239.1	39.98 ±0.24	681 ±2	77.6 ±0.4	21.1 ±0.2
Best	239.1	40.38	683	78.00	21.5

Except for lower fill factors (up to 0.8%), cells prepared on thin wafers display similar average cell parameters as in the case of cells prepared on standard thickness (170 μm) wafers shown in Table II. Best efficiencies up to 21.5 % could be achieved on full area of 239.1 cm^2 IBC cells on 130-μm thick wafers.

5 CONCLUSIONS

A seed layer and Cu-plating process for large area IBC cells has been investigated. Detailed analysis of sputtering damage caused by various layers has been performed. It is shown that even if the sputtering damage is present, it does not lie at the Si/SiO$_2$ interface and it could be masked by BBr$_3$ or POCl$_3$ duffused regions of the IBC cell. This damage does not cause any lifetime or J$_{0e}$ degradation on diffused samples and it can be effectively recovered by an anneal step. The developed seed layer and plating process has been integrated on large area IBC cells resulting in cells high effeicincy up to 21.9 % measured on full area of 239.1 cm^2.

6 ACKNOWLEDGEMENTS

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