

## ACHIEVEMENTS AND CHALLENGES TOWARDS HIGH EFFICIENCY, LARGE AREA IBC SOLAR CELLS

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Introduction

- IBC cell process flow
- Upscaling to full size devices
- Summary: Achievements & Challenges



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## INTERDIGITATED BACK CONTACT SILICON SOLAR CELLS



## **IBC: STATE-OF-THE-ART**

#### Industrial and semi-industrial homo-junction IBC cells

Reference	Year	Substrate	Area (cm <sup>2</sup> )	Eff. (%)
<sup>1</sup> D. Smith, SunPower	2014	CZ, n-type	155	24.5
<sup>1</sup> D. Smith, SunPower	2014	CZ, n-type	121	25.0
<sup>2</sup> C.B. Mo, Samsung SDI/Varian	2012	CZ, n-type	155	22.4
<sup>3</sup> A. Halm / J. Libal, ISC Konstanz / Silfab	2012	CZ, n-type	243	21.3
<sup>4</sup> Bosch / ISFH	2013	CZ, n-type	~240	22.1
<sup>5</sup> E. Franklin, ANU/Trina Solar	2014	CZ, n-type	~240	22.9

<sup>1</sup> D. Smith et al., 40<sup>th</sup> IEEE PVSC, Denver, USA (2014)

<sup>2</sup> C.B. Mo et al., 27<sup>nd</sup> EUPVSEC, Frankfurt, Germany (2012)

<sup>3</sup>A. Halm et al., 27<sup>nd</sup> EUPVSEC, Frankfurt, Germany (2012)

<sup>4</sup> Bosch SE, press release (2013)

<sup>5</sup> E. Franklin et al., SNEC, Shanghai, China (2014)

#### **IBC CELLS AT IMEC**

#### 2012:

Transfer of 2x2 cm<sup>2</sup> cells baseline from 4 inch FZ to **15.6** cm CZ substrates

#### 2013: **Stable baseline**, applied for new developments

- Innovation
- Process simplification
- Up scaling cell area
- Incorporation into module

2007: **IBC** research started at imec on p- and n-type 2011: Start of **IBC** platform

development:  $2x2 \text{ cm}^2$  cells on 4 inch n-type FZ substrates

## **BASELINE AT IMEC**

#### Wafers:

- I5.6xI5.6 cm<sup>2</sup> semi-square
- N-type Cz

## **Processing:**

- Diffusion
- Photolithography

## 

## Cells:

- 25 cells with an active area of 2x2 cm<sup>2</sup>
- Surrounded by test structures

## **IBC STATE-OF-THE-ART**

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#### Imec's small area IBC platform efficiencies

Reference	Year	Substrate	Area (cm²)	Eff. (%)
<sup>6</sup> M.Aleman, on 4 inch FZ	2012	FZ, n-type	4	23.3*
<sup>7</sup> O'Sullivan, on 156 mm CZ	2013	CZ, n-type	4	23.1*

\* Externally confirmed

<sup>6</sup> M. Aleman, et al., 2<sup>nd</sup> SiliconPV, Leuven, Belgium (2012);

<sup>7</sup> B.J. O'Sullivan, et al., 28<sup>th</sup> EUPVSEC, Paris, France (2013)



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## **BASELINE PROCESS CZ SILICON**



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B O'Sullivan et. al., Proc. EUPVSEC, (2013)

## LASER ABLATION FOR BSF DEFINITION

- **Basic laser parameters**
- Power
- Speed
- Continuous lines required
- Overlap between adjacent lines
- Additional optimization performed
- Emitter etch time after laser ablation





## LASER ABLATION: PROCESS DEVELOPMENT

#### Excessive laser speed/ insufficient line overlap



#### Insufficient laser power/line overlap



## Excessive overlap within one line



#### Optimum power and line overlap



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## **CONTACT HOLE DEFINITION**



- p<sup>+</sup> Si emitter
- Thermal SiO<sub>2</sub>
- On 10<sup>19</sup> cm<sup>-3</sup> Boron doped region
- n<sup>+</sup> Si BSF region
- Thermal SiO<sub>2</sub>
- On 10<sup>19</sup> cm<sup>-3</sup> Phosphorus doped region

## LASER ABLATED CONTACT HOLES



## Increased BSF contact

Reduced emitter contact

B O'Sullivan et. al., Proc. EUPVSEC, (2013)



## SCREEN PRINTING FOR METAL PATTERNING



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## **EFFECT OF BSF METAL WIDTH**



#### Paste control results in thinner BSF metal width

- Fill factor penalty results
- Fitting well with calculated trend line for photolitho case

## **DEVICE LEVEL**

#### Laser ablation

- BSF region definition
- Contact hole definition

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#### Screen printing

Metal patterning



Patterning method	J <sub>sc</sub> [mA/cm²]	V <sub>oc</sub> [mV]	FF [%]	Eta [%]
Photolithography	41.2	690	79.5	22.6
Ablation & Screen printing	41.3	687	78.5	22.2*

\* Externally confirmed

S Singh et. al., Proc. EUPVSEC, (2014)

## **SUMMARY: SMALL AREA CELLS**

#### Rear side patterning

- Emitter definition: laser ablation of oxide
- Contact opening: laser ablation of oxide
- Metal patterning: screen printing polymer paste

#### Photolitho-free best cell efficiency 22.2 %

Design rule defined: alignment accuracy vs losses



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  - Impact of cell area on characteristics
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#### Upscale cell design

Extend laser ablation and screen printing to full area

## **SUMMARY IV RESULTS**

	Area [cm²]	J <sub>sc</sub> [m <b>A</b> /cm²]	V <sub>oc</sub> [mV]	FF [%]	Eta [%]	# cells
Average	239	40.2	685	76.5	21.0	9
Best cell	239	40. I	686	77.4	21.3	

Promising  $J_{sc}$  and  $V_{oc}$  values FF limiting performance

## **IMPACT OF CELL AREA**

#### Best cell

Size [cm²]	Metal	J <sub>sc</sub> [mA/cm²]	V <sub>oc</sub> [mV]	FF [%]	η [%]
239	3 μm AlSi	40. I	686	77.4	21.3
4	$2\ \mu m$ AlSi	41.3	687	78.5	22.2*

 $V_{oc}$  independent of cell size  $J_{sc}$  and FF reduce with cell size

## INFLUENCE OF DESIGNATED ILLUMINATION APERTURE

(AND WHAT IT SHADES <sup>(2)</sup>)



Lower  $J_{sc}$  and FF when busbar's included

## FILL FACTOR LOSS ANALYSIS

Series resistance  $\Delta FF_{R_s} = \frac{J_{mpp}^2 R_s}{J_{sc} V_{oc}}$ Shunt resistance  $\Delta FF_{R_{sh}} = \frac{\left(V_{mpp} + J_{mpp}R_s\right)^2}{R_{sh} J_{sc} V_{oc}}$ 

 $\mathbf{J}_{02} \mathbf{loss} \qquad \qquad \Delta FF_{J_{02}} = FF_{J_{01}} - FF_0$ 

Additional busbar-induced loss  $\Delta FF_{BB} = pFF - FF - \Delta FF_{R_s}$ 

Allows decoupling of resistive loss mechanisms

A Khanna, IEEE J. Photovoltaics, (2013)

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B O'Sullivan, WC-PEC, (2014)



#### Series resistance loss is dominant



#### Resistive penalty for emitter BB inclusion



#### No significant impact on FF of BSF busbar



Significant series resistance losses present Additional emitter busbar-induced loss



Similar FF losses for small and large area cells

Series and Busbar resistances dominate

## **IMPACT OF BSF CONTACT DENSITY**



BSF contact resistance on indicates potential for FF improvement

30% higher density implemented

## **SERIES RESISTANCE**



Lateral non-uniformity in electroluminescence

Highest signal close to BSF contact point

Slight impact of increased grid density

Resistance dominated by BSF metal design



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## ACHIEVEMENTS

Laser ablation & polymer print processes developed

Large area IBC cells designed and fabricated

- Highest efficiency: 21.3 %
- Promising V<sub>oc</sub> and J<sub>sc</sub> values

Detailed analysis of fill factor losses

Framework for performance improvement

## **CHALLENGES**

Fill factor loss ...

- BSF metal width / paste control trade-off
- Dependence on distance from contact point

Move towards module compatible metallisation

Cu plating development ongoing



# Thank you for your attention !

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