Strategies for ultra-low Ag consumption of industrial n-type cells

L.J. Geerligs[1,a], M.W.P.E. Lamers[1,b], A.R. Burgers[1,c], M. Dovrat[2,d],

G. Eytan[2,e], J. Bertens[3,f], M. Kivits[3,g], B. O'Sullivan[4,h], M. Debucquoy[4,i]

[1]ECN Solar Energy, P.O. Box 1, NL-1755 ZG Petten, the Netherlands
[2]Xjet Ltd., 10 Oppenheimer St., Rehovot 76701, Israel
[3]Meco Equipment Engineers B.V., Marconilaan 2, 5151 DR Drunen, The Netherlands
[4]IMEC, Kapeldreef 75, 3001 Leuven, Belgium
[a]geerligs@ecn.nl, [b]lamers@ecn.nl, [c]burgers@ecn.nl, [d]Miki.Dovrat@xjetsolar.com,
[e]Guy.Eytan@xjetsolar.com, [f]jurgen.bertens@besi.com, [g]marc.kivits@besi.com,
[h]Barry.Osullivan@imec.be, [i]Maarten.Debucquoy@imec.be

Abstract: For cost reduction as well as reduction of environmental footprint of solar cells, it is important to reduce the use of silver (Ag) in metallisation. In this work we report on large reduction of Ag consumption for industrial high-efficiency bifacial n-type cells with front and rear Ag grid, by modest process changes. Both front-and-rear contacted, as well as metal-wrap-through cells, are considered.
The approaches explored are, for the front, seeding with a small amount of Ag fire-through ink or paste, and plate the thus formed contact grid with copper (Cu). For the rear we use the same approach, or replace the Ag grid by an Al layer. Front Ag consumption of 10mg per wafer and rear Ag consumption of 20mg per wafer were demonstrated for inkjet seeding. The front finger width after inkjet seed&plate is about 55um. With screen print or stencil print seeding a significant Ag reduction can be obtained too, but not to the same level as with inkjet printing.
The replacement of a rear Ag grid by an Al contact layer deposited by physical vapour deposition requires optimisation of the rear dielectric in order to obtain good rear internal reflection. We model and experimentally demonstrate that a small modification of the rear dielectric already yields an acceptable reflection.
In all experiments we find approximately equal or better efficiency than in the reference process; and also the cost of ownership estimates are favorable. This shows that a better environmental footprint can be well combined with improved production cost.
Keywords: copper plating, crystalline silicon, n-type cells, n-PERT.

1 Introduction

High efficiency, ease of industrialization and reliability are the main drivers towards low-cost (€/Wp) Silicon PV. The International Technology Roadmap for PV version 2014 expects the share of n-type cell technology to reach 40% in 2024, and of rear contact cells to reach slightly over 20% in 2024. In accordance with these trend, ECN has developed industrial bifacial n-type front and rear contact (n-Pasha) [1] and n-type rear contact Metal-Wrap-Through (n-MWT) technologies. ECN's n-MWT technology offers significant cell and module performance gain over n-Pasha in a cost-effective way [2]. With only modest changes to the n-Pasha production process, the n-MWT technology reproducibly increases the performance: up

to 0.3% abs. efficiency gain at cell level and up to 3% power gain at module level have been demonstrated (up to 5% module power gain anticipated). A full size module made using n-MWT cells of 19.6% average efficiency resulted in a power output close to 280W (despite some Isc-mismatch). To place in perspective, with cell efficiency over 20%, a full area n-MWT module efficiency above 18.5% is expected. More recent cell and module results for the n-MWT technology, with cell efficiency upto 20.5%, are reported in another paper at this conference [3]. ECN's MWT module technology is based on an integrated conductive backsheet (CBS) which results in higher yield and reduced interconnection-process-related stress, allowing use of (much) thinner cells and therefore offering additional cost reduction possibilities.

The n-Pasha and n-MWT cells are metallised by screen printed silver (Ag) pastes. For cost reduction and as well as reduction of environmental footprint of solar cells, it is important to reduce the use of Ag in metallisation. In this work we report on large reduction of Ag consumption for industrial high-efficiency bifacial n-type cells with front and rear Ag grid, by modest process changes. Both front-and-rear contacted, as well as metal-wrap-through cells, are considered. The approaches explored are, for the front, seeding with a small amount of Ag fire-through ink or paste, and plate the thus formed contact grid with copper (Cu). For the rear we use the same approach, or replace the Ag grid by an Al layer deposited by physical vapour deposition. In all experiments we find approximately equal or better efficiency than in the reference process; and also the cost of ownership estimates are favorable. This shows that a better environmental footprint can be well combined with improved production cost

2 Cell process

The n-type cell process is similar to the industrial process used for ECN's n-Pasha and Yingli Solar's Panda cells (Pasha= bifacial cell design with passivated front and rear side and with H-pattern contact grids). The standard cell structure comprises a boron emitter, a phosphorous Back Surface Field (BSF) and an open rear side metallization, and is thus suitable for thin wafers. In this work we report results for n-MWT cells downto 150μm thickness, and in [3] results for n-MWT cells downto 120μm thickness are reported. The front and rear side metal grid patterns are based on a H-pattern grid design.

For these proof-of-principle experiments on reduction of Ag consumption, we have used material and cell processing without particularly aiming for high efficiency, and as a result the average efficiencies are comparatively low. However, the results from these experiments are just as representative for, and can be just as well applied to, high efficiencies. Experiments aiming at efficiency >20% are ongoing.

The approaches we explore for Ag reduction are, for the front, seeding with a small amount of Ag fire-through ink or paste, and plate the thus formed contact grid with copper (Cu). For the rear we use the same approach, or replace the Ag grid by a sputtered Al layer. The implementation of seed&plate should be relatively straightforward in production, basically only adding a plating tool, and perhaps changing (a) printer(s).

The replacement of the rear Ag grid by an Al layer involves more significant changes from the normal process flow, adding several tools after the front print&fire steps.

3 Results

3.1 Front seed & plate

n-Pasha cells were metallised on the front with inkjet seed patterns of between 9.8 and 13 mg of Ag, and on the rear with the regular screen printed grid. The Ag consumption in the front busbars was not optimised yet, and can probably be reduced further. The front side was plated with Ni, followed by 8 µm of Cu, and a capping layer, to a line resistance of approx. 0.4 Ohm/cm. Fig. 1 shows an image of a plated finger of 54 µm average width. Unfortunately, not all fingers were the same width, depending on calibration of the inkjet process some fingers had increased width which decreased the Isc. Also, the firing optimisation of the front seed is possibly not yet satisfactory, resulting in a lower FF than should optimally be possible. Table 1 shows cell I-V results. In G4 the spread in FF was large, but some cells had FF above 79%, better than the reference. We aim to improve the process to reach more uniform performance, and performance which is equal to the reference. Overall the efficiency of the seed&plate groups is slightly below the reference, which is due to the Isc loss. It will be attempted to avoid this in future experiments by improved inkjet process parameters.

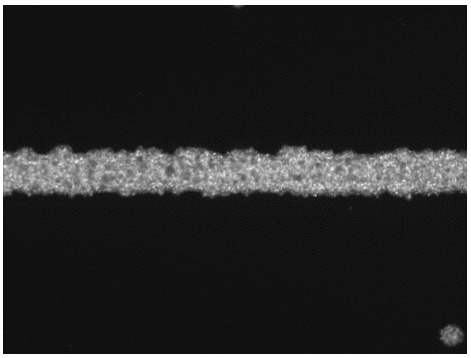

Figure 1. Image of inkjet seed & Cu plate finger of the front grid.

Seed	Isc (A) Area=239cm^2	Voc (V)	FF (%)	eta (%)
Reference (no seed)	9.065 ±0.04	0.6320* ±0.003	78.59* ±0.8	18.88 ±0.2
G1: 13.3mg	8.899 ±0.04	0.6332 ±0.003	78.67 ±0.5	18.56 ±0.1
G2: 13.3mg	8.936 ±0.02	0.6323 ±0.001	78.62 ±1.4	18.61 ±0.4
G3: 11.5mg	8.974 ±0.06	0.6334 ±0.0003	78.57 ±1.0	18.72 ±0.4
G4: 9.8mg	8.969 ±0.01	0.6336 ±0.0009	75.6 ±3	17.98 ±0.7

Table 1. I-V results of groups with different front side seed grids (differing in amount of Ag used for the seeding). All groups consist of about 8 cells. Values given are median ± standard deviation.

3.2 Rear seed & plate

With rear seed&plate there is the benefit of FF improvement and Ag reduction, and no risk of Isc reduction such as might happen for seed&plate of the front side of the cell. Therefore it is more straightforward to reach increased efficiency compared to reference. Also ghost plating, if any, will not be visible in a module. In early experiments we have reached Ag consumption down to 20mg for rear seed with inkjet, but those seeds were combined with a non-optimised plating process, resulting in a lower efficiency than the reference group (the same efficiency

reduction due to the plating occurred in that experiment for a group with a screen printed seed grid). After optimisation of the plating process, the rear seed&plate approach has been tested so far only with a screen printed seed grid. Results are given in Table 2.

Seed	Isc (A) Area=239cm^2	Voc (V)	FF (%)	eta (%)
Reference (no seed)	8.88 ± 0.02	0.632 ± 0.001	78.9 ± 0.15	18.51± 0.06
Plate 8μm Cu	8.89 ± 0.02	0.633 ± 0.001	79.0 ± 0.16	18.59 ± 0.06
Plate 16μm Cu	8.89 ± 0.04	0.633 ± 0.001	79.0 ± 0.17	18.55 ± 0.07

Table 2. I-V results for rear screen printed seed and plate. All groups consist of about 8 cells. Values given are median ± standard deviation.

The FF gain *expected* for the 8μm and 16μm plated groups, based on the reduction of the grid resistance, would be 0.2% and 0.4%, respectively. The results don't clearly demonstrate this gain. Experiments are continuing to optimise this gain, or understand why it is absent, and to again include inkjet printed rear seed grids.

3.3 Seed & plate of Metal-Wrap-Through cells

In addition to n-Pasha cells, also n-type MWT cells have been plated on the front, the rear, and both sides, to investigate any possible differences compared to n-Pasha cells. The same plating process can be used for n-type MWT cells as for n-Pasha cells. One notable advantage in the MWT case is that for capping of the Cu plating layer, an organic solder preservative can be used (OSP). This is compatible with the subsequent CBS-based module process. We have reported on this in ref [4].

The plating results for n-MWT cells appear to be very comparable to those for n-Pasha cells. Cells with a thickness of 150μm were plated without any problems. A slight but acceptable increase of current under reverse bias occurs. Results for cells of 150μm and 180μm thickness are shown in Fig. 3. We note that typical Irev for n-MWT cells is below 0.3A, but for this experiment n-MWT cells with a range of Irev were selected to observe the possible impact of the plating.

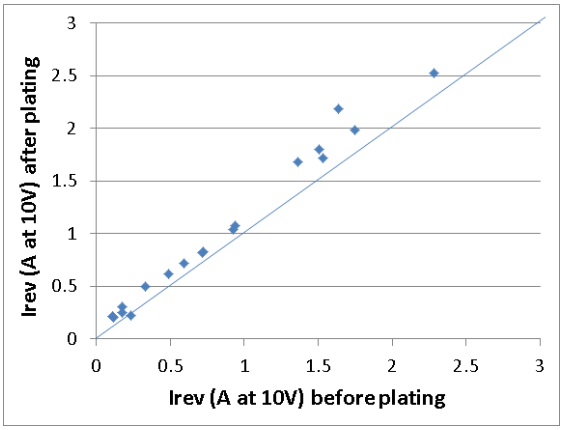

Figure 3. Reverse current change upon plating of n-MWT cells with fire-through seed. Cells with a range of Irev were selected. Note that the typical Irev for n-MWT cells is below 0.3A.

Because the initial experiments were performed with standard cells (no special seed grids), with additional front busbars to connect to the electrical contacts for plating (see Fig. 4), cell efficiency results are not really informative in this case. The cells that were plated on the rear side only, showed a FF-increase of 0.5%$_{abs}$ (efficiency increase of slightly larger than 0.1%$_{abs}$) despite the fact that a standard grid was used as seed. This is somewhat surprising given the absence of the expected FF-gain for the rear-plated n-Pasha cells in Table 2. Module reliability tests with these cells are ongoing, and will be reported elsewhere.

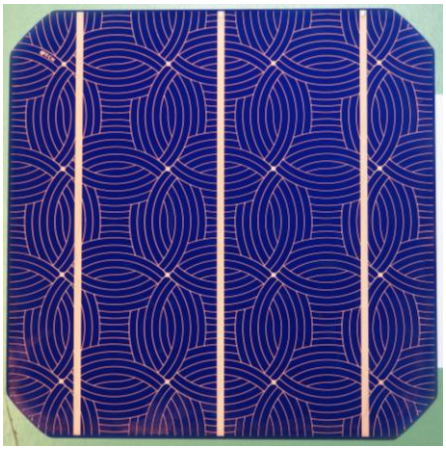

Figure 4. Photograph of Cu-plated n-type MWT cell with 16 via's. The three busbars would normally not be present in the MWT grid, but were in this case added as an improvised means to connect to the electrical contacts for the plating.

3.4 Al rear side metallisation

Al is a well-known contacting material for silicon devices, including solar cells. If it is processed at low temperature (to avoid alloying), it can be used to contact the n+ doped rear side of the n-type cells. When the front side is contacted by a fire-through grid, this means that after firing the rear side dielectric should be opened, followed by Al PVD (physical vapour deposition). We have investigated various lasers and laser settings and grid designs for opening the rear dielectric, with open fractions downto 0.05%. Results of initial tests are given in Table 3.

Laser opening area (% of wafer area)	**Isc (A) Area=239cm^2**	**Voc (V)**	**FF (%)**	**eta (%)**
G1: Reference (print&fire rear grid)	9.16 ± 0.01	0.631 ± 0.001	77.5 ± 0.8	18.74± 0.16
G2: contact area 9%	9.00 ± 0.001	0.638 ± 0.001	78.7 ± 0.05	18.90 ± 0.04
G3: contact area 9%	9.00 ± 0.05	0.638 ± 0.002	78.7 ± 0.04	18.79 ± 0.17
G4: contact area 0.36%	8.98 ± 0.03	0.636 ± 0.0003	78.1 ± 0.9	18.71 ± 0.26
G5: contact area 0.05%	8.99 ± 0.02	0.637 ± 0.001	75.3 ± 1.7	18.02 ± 0.43

Table 3. I-V results for n-type front emitter cells with rear Al-PVD metallisation, compared to a reference group with rear fire-through grid (n-Pasha design). G2-G5 have used different laser types and laser settings, where the settings of G2 and G3 apparantly gave least damage, but were not yet tested at small open fractions. Group size is 3 cells. Values given are median ± standard deviation.

The contacting by Al instead of a fire-through grid results in a Voc-gain of 6-7mV, and a FF-gain of upto 0.5-1.0%. Even for small contact area there is increase of FF, and we estimate the contact resistance to be about or below 0.3 $m\Omega cm^2$. However there is an Isc reduction of about 1.5%, so that the efficiency gain is only upto about 0.1-0.2%abs.

The reason for the drop in Isc is concluded from Fig. 5 to be related to rear-side internal reflection.

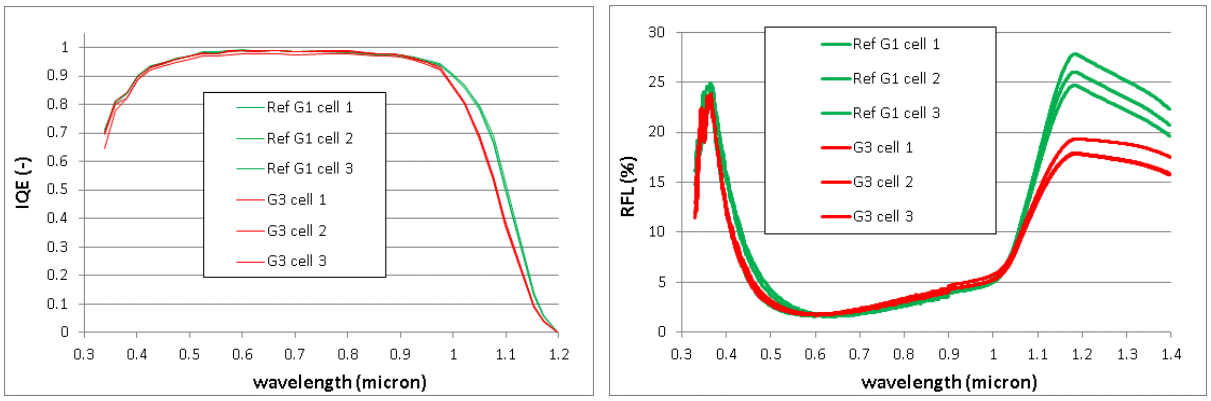

Figure 5. Internal quantum efficiency and front escape reflectance of n-type cells with Ag fire-through grid and n-type cells with Al-PVD rear metallisation.

We have investigated routes to improve the rear internal reflection. One approach investigated is to add a thin layer of SiOx on top of the usual SiNx rear side coating. Fig. 6 shows the effect of adding an SiOx layer between the SiNx and the Aluminium contact layer. Fig. 6a gives from modeling the hemispherically averaged value for a single internal rear reflection. Fig. 6b gives the actual escape reflectance, tested on samples without diffused layers. Because of the absence of the diffused layers there is much less free carrier absorption, therefore the escape reflectance is much higher than in Fig. 5.

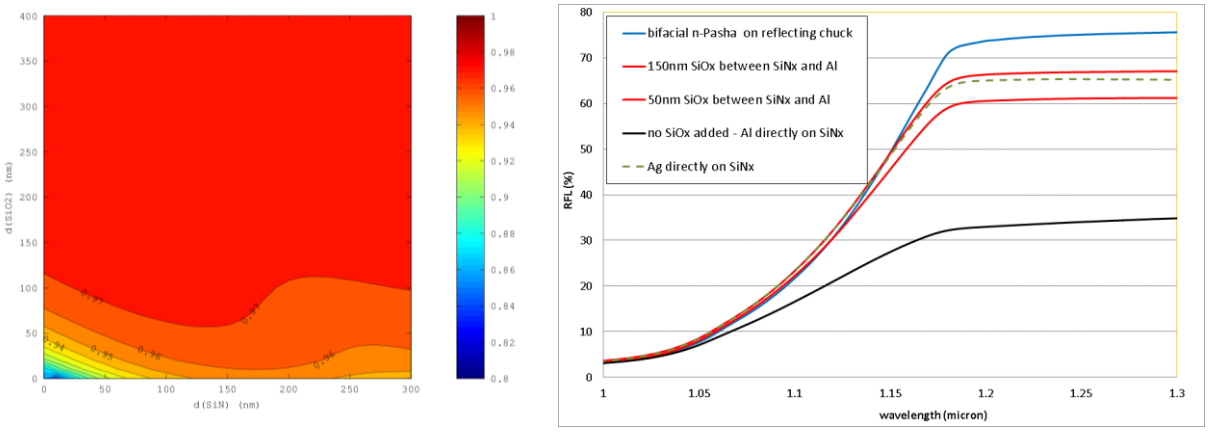

Figure 6. a (Left): Calculated internal rear reflectance for a layer of SiOx (vertical axis = SiOx thickness) between SiNx (horizontal axis = SiNx thickness) and Aluminium. b (Right): experimental result for escape reflection for different rear side stacks. The red curves (SiOx added) compared to the black curve (no SiOx added, situation of Table 3 and Fig. 3) show how adding 50nm or 150nm of SiOx brings the escape reflection close to the blue curve, representing the bifacial n-Pasha situation. For comparison, also the effect of a Ag reflector deposited directly on a SiNx rear dielectric is shown.

Initial experiments at cell level with the rear dielectric for improved rear reflection are shown in Table 4. The Al metallisation process was different from the pre-experiment (different tools and different process conditions)[5]. The Isc is now indeed at the same level as for the reference, but in this experiment the FF is reduced for the Al metallisation. Also the gain in Voc is absent in this case. The improvement of Isc is in our opinion in agreement with the simulations and tests of Fig. 6, and we expect the Voc and FF gains from the experiment of Table 3 can be recovered by process optimisation.

Dielectric	Isc (A) Area=239cm^2	Voc (V)	FF (%)	eta (%)
G1: Reference (print&fire rear grid)	9.24 ± 0.04	0.644 ± 0.002	78.6 ± 0.5	19.54± 0.13
G2: 50nm SiOx added	9.25 ± 0.04	0.644 ± 0.002	77.0 ± 0.11	19.19 ± 0.3
G3: 150nm SiOx added	9.22 ± 0.05	0.644 ± 0.002	77.0 ± 0.07	19.09 ± 0.16

Table 4. I-V results for n-type front emitter cells with rear Al-PVD metallisation, compared to a reference group with rear fire-through grid (n-Pasha design). Group size is 6 cells. Values given are median ± standard deviation.

4 Summary

We have investigated routes to reduce Ag consumption in n-type front and rear contact and n-type MWT cells. The option of fire-through Ag seed print followed by Ni/Cu plating gives good results, with similar efficiency as the reference process. There is potential for FF-increase, although this is not always born out by the experiments so far. The potential for Ag reduction is large, in particular in the case of inkjet print for seed pattern, where about 10 mg per wafer side is proven to be feasible. As usual for seed and plate, the challenge for the front side is to maintain a high Isc; this appears to be well feasible when using inkjet seed print (although due to instrumental artifacts we still see a slight loss in the experiments reported here). Finally, a more drastic deviation from standard industrial processing is to use Al pvd for rear side metallisation. This shows good Voc and FF gain (although not in all our experiments so far). The rear side dielectric needs a relatively minor adjustment (for example, adding a thin layer of SiOx) to avoid loss in Isc due to reduced rear side internal reflection.

5 Acknowledgments

The research leading to these results has received funding from the European Union's Seventh Programme for research, technological development and demonstration under grant agreement No 308350. This paper reflects only the authors' views and the European Union is not liable for any use that may be made of the information contained herein.

References

[1] I.G. Romijn et al., 27th EU-PVSEC, 2012
[2] N. Guillevin et al., 27th EU-PVSEC, 2012
[3] N. Guillevin et al., this conference.
[4] I. Bennett et al., Photovoltaics International, 21st edition, 2013, pp. 100 – 106.
[5] Al deposition in ATON tool, courtesy Applied Materials