STRATEGIES FOR ULTRA-LOW AG CONSUMPTION OF INDUSTRIAL N-TYPE CELLS

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ABSTRACT: For cost reduction as well as reduction of environmental footprint of solar cells, it is important to reduce the use of silver (Ag) in metallisation. In this work we report on large reduction of Ag consumption for industrial high-efficiency bifacial n-type cells with front and rear Ag grid, by modest process changes. Both front-and-rear contacted, as well as metal-wrap-through cells, are considered.
The approaches explored are, for the front, seeding with a small amount of Ag fire-through ink or paste, and plate the thus formed contact grid with copper (Cu). For the rear we use the same approach, or replace the Ag grid by a Al layer deposted by physical vapour deposition (PVD). Front Ag consumption of 10mg per wafer and rear Ag consumption of 20mg per wafer were demonstrated for inkjet seeding. The front finger width after inkjet seed&plate is about 55µm. With screen print or stencil print seeding a significant Ag reduction can be obtained too, but not to the same level as with inkjet printing.
The replacement of a rear Ag grid by an Al contact layer deposited by PVD requires optimisation of the rear dielectric in order to obtain good rear internal reflection. We model and experimentally demonstrate that a small modification of the rear dielectric already yields an acceptable reflection.
In all experiments we find approximately equal or better efficiency than in the reference process; and also the cost of ownership estimates are favorable. This shows that a better environmental footprint can be well combined with improved production cost.
Keywords: back-contact, bifacial, n-type, c-Si, cost reduction, sustainable, metallization

1 INTRODUCTION

High efficiency, ease of industrialization and reliability are the main drivers towards low-cost (€/Wp) Silicon PV. The International Technology Roadmap for PV version 2014 expects the share of n-type cell technology to reach 40% in 2024, and of rear contact cells to reach slightly over 20% in 2024. In accordance with these trend, ECN has developed industrial bifacial n-type front and rear contact (n-Pasha) [1] and n-type rear contact Metal-Wrap-Through (n-MWT) technologies. ECN's n-MWT technology offers significant cell and module performance gain over n-Pasha in a cost-effective way [2,3]. With only modest changes to the n-Pasha production process, the n-MWT technology reproducibly increases the performance: 0.3% abs. efficiency gain or more (depending on grid design) at cell level and up to 3% power gain at module level have been demonstrated (up to 5% module power gain anticipated). Recent cell and module results for the n-MWT technology, with cell efficiency up to 21%, and module power over 300W, are reported in another paper at this conference [3]. ECN's MWT module technology is based on an integrated conductive backsheet (CBS) which results in higher yield and reduced interconnection-process-related stress, allowing use of (much) thinner cells and therefore offering additional cost reduction possibilities.

The n-Pasha and n-MWT cells are metallised by screen printed silver (Ag) pastes. For cost reduction as well as reduction of environmental footprint of solar cells, it is important to reduce the use of Ag in metallisation. Good progress has been made in recent years by fine line printing. In principle large reduction of Ag consumption is possible by very fine line printing and use of several rows of contacts (e.g. 4 or 5 busbars, or 6x6 vias in an MWT cell [3]). Figure 1 illustrates the possible advantage for reduction of metallisation mass from (quite generalized) modeling. However, it is challenging to realise such a reduction in practice since it requires printing of very fine (narrow and thin) lines with uniform properties.

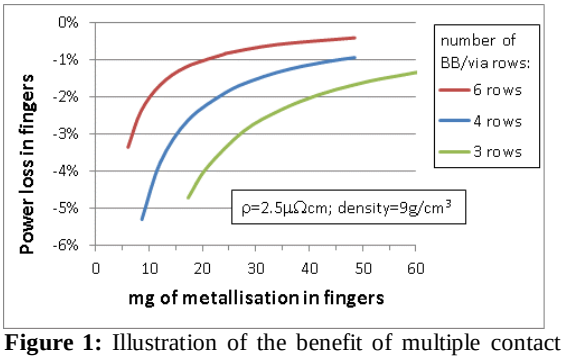

Figure 1: Illustration of the benefit of multiple contact rows (i.e., busbars, or vias in the case of MWT cells) for paste reduction potentiality. Figures apply to one cell side.

In this work we report on large reduction of Ag consumption for industrial high-efficiency bifacial n-type cells with front and rear Ag grid, by other approaches, requiring only modest changes from normal production. Both front-and-rear contacted, as well as metal-wrap-through cells, are considered. The approaches explored are, for the front, seeding with a small amount of Ag fire-through ink or paste, and plate the thus formed contact grid with copper (Cu). For the rear we use the same approach, or replace the Ag grid by an Al layer deposited by physical vapour deposition. In all experiments we find approximately equal or better efficiency than in the reference process; and also the cost of ownership estimates are favorable. This shows that a better environmental footprint can be well combined with

improved production cost. Similar work was recently reported by Kraft et al. in [4].

2 EXPERIMENTAL

2.1 Cell process

The n-type cell process is similar to the industrial process used for ECN's n-Pasha cells (Pasha= bifacial cell design with passivated front and rear side and with H-pattern contact grids). The standard cell structure comprises a boron emitter, a phosphorous Back Surface Field (BSF) and an open rear side metallization, and is thus suitable for thin wafers. The front and rear side metal grid patterns are based on a H-pattern grid design. A metal-wrap-through (MWT) variation of the cell has also been developed, which yields higher efficiencies (0.15-0.3%abs higher for 16 vias) than the front-and-rear-contacted cell. So far this cell process has resulted in efficiencies near 20.5% for the n-Pasha and 21% for the MWT version of the cell [3].

For these proof-of-principle experiments on reduction of Ag consumption, we have used material and cell processing without particularly aiming for high efficiency, and as a result the average efficiencies are comparatively low. However, the results from these experiments are just as representative for, and can be just as well applied to, high efficiencies.

The approaches we explore for Ag reduction are, for the front, seeding with a small amount of Ag fire-through ink or paste, and plate the thus formed contact grid with copper (Cu). For the rear we use the same approach, or replace the Ag grid by a sputtered Al layer. The implementation of seed&plate should be relatively straightforward, basically only adding a plating tool, and perhaps changing (a) printer(s).

The replacement of rear Ag grid by a sputtered Al layer involves perhaps more significant changes from the normal process flow, adding several tools after the front print&fire steps.

2.2 Front seed and plate

n-Pasha cells were metallised on the front with inkjet seed patterns of between 9.8 and 13 mg of Ag, and on the rear with the regular screen printed grid. The Ag consumption in the front busbars was not optimised yet, and can probably be reduced further. The front side was plated with Ni, followed by 8 µm of Cu, and a capping layer, to a line resistance of approx. 0.4 Ω/cm. Fig. 2 shows an image of a plated finger of 54µm average width. Unfortunately, not all fingers were the same width: depending on calibration of the inkjet process some fingers had increased width which decreased the Isc. Also the firing optimisation of the front seed is possibly not yet satisfactory, resulting in a lower FF than should optimally be possible. Table I shows cell I-V results. In G4 the spread in FF was large, but some cells had FF above 79%, better than the reference. We expect the process can be improved to reach more uniform performance, and performance which is equal to the reference. Overall the efficiency of the seed&plate groups is slightly below the reference, which is due to the Isc loss. By improved inkjet process parameters this Isc loss could be avoided.

The Ag consumption of order 10mg is similar to the results published by Kraft et al. in [4], for front side seeding of p-type cells with screen printing.

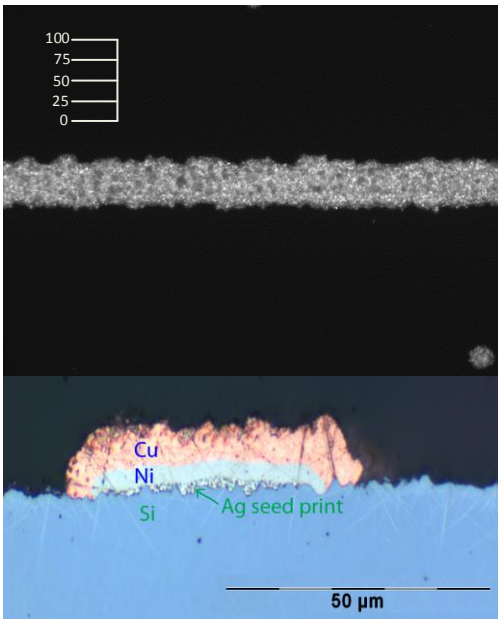

Figure 2: Top: Image of inkjet seed & Cu plate finger of the front grid. Bottom: cross section. Seed print Ag mass was in this case 2.4mg for the grid fingers.

Table I: I-V results of groups with different front side seed grids (differing in amount of Ag used for the seeding). All groups consist of about 8 cells. Values given are median ± standard deviation. Cell area is 239cm^2.

Seed	**Isc (A)**	**Voc (V)**	**FF (%)**	**η (%)**
Reference (no seed)	9.07 ±0.04	0.632 ±0.003	78.6 ±0.8	18.9 ±0.2
G1: 13.3mg Ag	9.00 ±0.04	0.633 ±0.003	78.7 ±0.5	18.6 ±0.1
G2: 13.3mg Ag	8.94 ±0.02	0.632 ±0.001	78.6 ±1.4	18.6 ±0.4
G3: 11.5mg Ag	8.97 ±0.06	0.633 ±0.0003	78.6 ±1.0	18.7 ±0.4
G4: 9.8mg Ag	8.97 ±0.01	0.634 ±0.0009	75.6 ±3	18.0 ±0.7

2.3 Rear seed and plate

With rear seed&plate there is the benefit of FF improvement and Ag reduction, and no risk of Isc reduction such as might happen for seed&plate of the front side of the cell. Therefore it is more straightforward to reach increased efficiency compared to reference. Also ghost plating, if any, will not be visible in a module. In early experiments we have reached Ag consumption down to 12mg for rear seed with inkjet, but those seeds were combined with a non-optimised plating process, resulting in a lower efficiency than the reference group (the same efficiency reduction due to the plating occurred in that experiment for a group with a screen printed seed grid). After optimisation of the plating process, the rear seed&plate approach has been tested so far only with a screen printed seed grid. Results are given in Table II.

The FF gain expected for the 8µm and 16µm plated groups, based on the reduction of the grid resistance, is

0.2% and 0.4%, respectively. The results don't clearly demonstrate this gain. It is unclear what the reason is; later similar experiments on MWT cells did show approximately the expected FF gain.

Table II: I-V results for rear screen printed seed and plate. All groups consist of about 8 cells. Values given are median ± standard deviation. Cell area is 239 cm^2.

Seed	Isc (A)	Voc (V)	FF (%)	η (%)
Reference (no seed)	8.88 ± 0.02	0.632 ± 0.001	78.9 ± 0.15	18.51± 0.06
Plate 8µm Cu	8.89 ± 0.02	0.633 ± 0.001	79.0 ± 0.16	18.59 ± 0.06
Plate 16µm Cu	8.89 ± 0.04	0.633 ± 0.001	79.0 ± 0.17	18.55 ± 0.07

2.4 Seed and plate of metal-wrap-through cells

In addition to n-Pasha cells, also n-type MWT cells have been plated on the front, the rear, and both sides, to investigate any possible differences compared to n-Pasha cells. The same plating process can be used for n-type MWT cells. One notable advantage in the MWT case is that for capping of the Cu plating layer, an organic solder preservative can be used (OSP). We have reported on this earlier [5]. However, since then we have found that in Damp Heat module reliability tests some FF degradation occurs and we suspect this may be related to the use of the OSP. If so, perhaps a less "agressive" OSP can avoid this issue, otherwise an alternative capping layer such as Sn can be used.

The plating results for n-MWT cells appear to be very comparable to those for n-Pasha cells. A slight but acceptable increase of current under reverse bias occurs, which is probably related to plating of the metallisation around the via.

Because the initial experiments were performed with standard cells (no special seed grids), with additional front busbars to connect to the electrical contacts for plating (see Fig. 3), cell efficiency results are not really informative in this case. Module reliability tests with these cells are ongoing, and will be reported elsewhere. Apart from the FF degradation under Damp Heat test mentioned above, the reliability tests, so far upto 2000 hours Damp Heat and 400 Thermal Cycles, give good results.

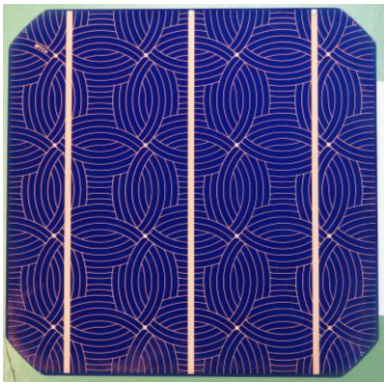

Figure 3: Photograph of Cu-plated n-type MWT cell with 16 vias. The three busbars would normally not be present in the MWT grid, but were in this case added as an improvised means to connect to the electrical contacts for the plating.

2.5 Al rear side metallisation

Al is a well-known contacting material for silicon devices, including solar cells. If it is processed at low temperature (to avoid alloying), it can be used to contact the n+ doped rear side of the n-type cells. When the front side is contacted by a fire-through grid, this means that after firing the rear side dielectric should be opened, followed by Al PVD (physical vapour deposition). We have investigated various lasers and laser settings and grid designs for opening the rear dielectric, with open fractions downto 0.05%. Results of these tests are given in Table III.

Table III: I-V results for n-type front emitter cells with rear Al-PVD metallisation, compared to a reference group with rear fire-through grid (n-Pasha design). G2-G5 have used different laser types and laser settings, where the settings of G2 and G3 apparently gave least damage, but were not yet tested at small open fractions. Group size is 3 cells. Values given are median ± standard deviation.

Laser opened area	Isc (A)	Voc (V)	FF (%)	η (%)
G1: Reference (print&fire rear grid)	9.16 ± 0.01	0.631 ± 0.001	77.5 ± 0.8	18.74± 0.16
G2: contact area 9%	9.00 ± 0.001	0.638 ± 0.001	78.7 ± 0.05	18.90 ± 0.04
G3: contact area 9%	9.00 ± 0.05	0.638 ± 0.002	78.7 ± 0.04	18.79 ± 0.17
G4: contact area 0.36%	8.98 ± 0.03	0.636 ± 0.0003	78.1 ± 0.9	18.7 ± 0.3
G5: contact area 0.05%	8.99 ± 0.02	0.637 ± 0.001	75.3 ± 1.7	18.0 ± 0.4

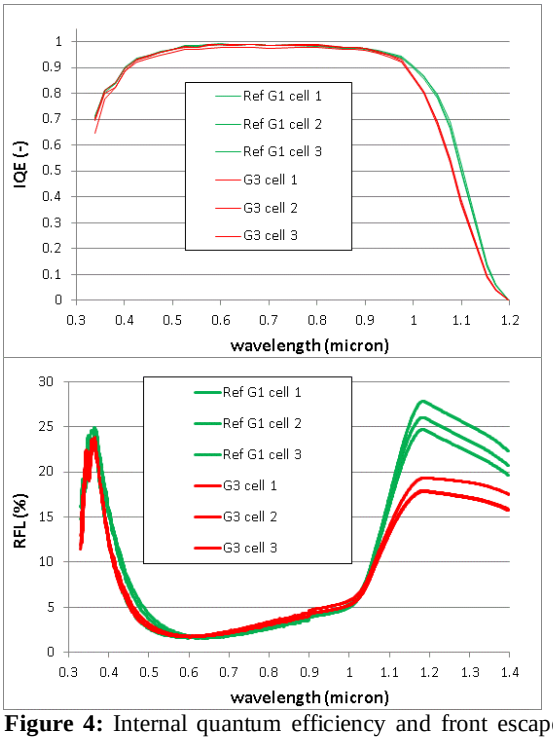

Figure 4: Internal quantum efficiency and front escape reflectance of n-type cells with Ag fire-through grid and n-type cells with Al-PVD rear metallisation

The contacting by Al instead of a fire-through grid results in a Voc-gain of 6-7mV, and a FF-gain of upto 0.5-1.0%. Even for small contact area there is increase of FF, and we estimate the contact resistance to be about or below 0.3 $m\Omega cm^2$. However there is an Isc reduction of about 1.5%, so that the efficiency gain is only upto about 0.1-0.2%abs.

The reason for the drop in Isc is concluded from Fig. 4 to be related to rear-side internal reflection.

We have investigated routes to improve the rear internal reflection. One approach investigated is to add a thin layer of SiOx on top of the usual SiNx rear side coating. Fig. 5 shows the effect of adding an SiOx layer between the SiNx and the Aluminium contact layer. The actual escape reflectance given in Fig. 5 was obtained from samples without diffused layers. Because of the absence of the diffused layers there is much less free carrier absorption, therefore the escape reflectance is much higher than in Fig. 4.

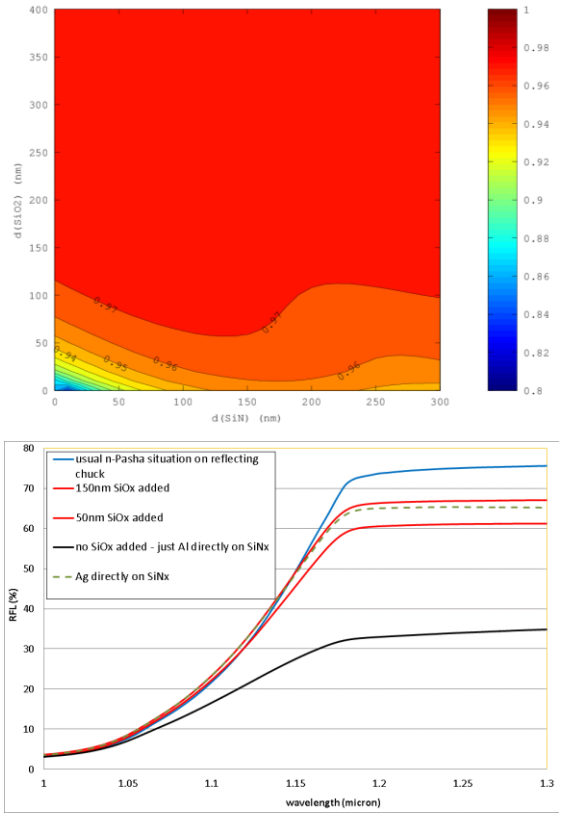

Figure 5: (top): Calculated internal rear reflectance for a layer of SiOx (vertical axis = SiOx thickness) between SiNx (horizontal axis = SiNx thickness) and aluminium. Shown is the hemispherically averaged value for a single internal rear reflection. (bottom): Experimental result for escape reflection for different rear side stacks. The red curves (SiOx added) compared to the black curve (no SiOx added, situation of Table 3 and Fig. 3) show how adding 50nm or 150nm of SiOx brings the escape reflection close to the blue curve, representing the bifacial n-Pasha situation. For comparison, also the effect of a Ag reflector deposited onto the usual SiNx rear dielectric is shown.

Initial experiments at cell level with the rear dielectric for improved rear reflection are shown in Table IV. The Al metallisation process was different from the pre-experiment (different tools and different process conditions) [6]. The Isc is now indeed at the same level as for the reference, but in this experiment the FF is reduced for the Al metallisation. Also the gain in Voc is absent in this case. The improvement of Isc is in our opinion in agreement with the simulations and tests of Fig. 5, and we expect the Voc and FF gains from the experiment of Table III can be recovered by process optimisation

Table IV: I-V results for n-type front emitter cells with rear Al-PVD metallisation, compared to a reference group with rear fire-through grid (n-Pasha design). Group size is 6 cells. Values given are median ± standard deviation.

Dielectric	Isc (A)	Voc (V)	FF (%)	η (%)
G1: Reference (print&fire rear grid)	9.24 ± 0.04	0.644 ± 0.002	78.6 ± 0.5	19.54± 0.13
G2: 50nm SiOx added	9.25 ± 0.04	0.644 ± 0.002	77.0 ± 0.11	19.2 ± 0.3
G3: 150nm SiOx added	9.22 ± 0.05	0.644 ± 0.002	77.0 ± 0.07	19.09 ± 0.16

3 CONCLUSIONS

We have investigated routes to reduce Ag consumption in n-type front and rear contact, and n-type MWT cells. The option of fire-through Ag seed print followed by Ni/Cu plating gives good results, with similar efficiency as the reference process. There is potential for FF-increase, although this is not always born out by the experiments so far. The potential for Ag reduction is large, in particular in the case of inkjet print for seed pattern, where about 10 mg per wafer side is proven to be feasible. As usual for seed and plate, the challenge for the front side is to maintain a high Isc; this appears to be well feasible when using inkjet seed print (although due to instrumental artifacts we still see a slight loss in the experiments reported here). Finally, a more drastic deviation from standard industrial processing is to use Al PVD for rear side metallisation. This shows good Voc and FF gain (although not in all our experiments so far). The rear side dielectric needs a relatively minor adjustment (for example, adding a thin layer of SiOx) to avoid loss in Isc due to reduced rear side internal reflection

3 ACKNOWLEDGMENTS

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4 REFERENCES

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