Application of seed and plate metallization to 15.6cm × 15.6cm IBC cells

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ABSTRACT

Interdigitated back contact (IBC) Si solar cells can be highly efficient: record efficiencies of up to 25.0%, measured over a cell area of 121cm², have been demonstrated on IBC solar cells by SunPower. The high efficiencies achieved can be attributed to several advantages of cells of this type, including the absence of front metal grid shading and a reduced series resistance. Several metallization schemes have been reported for IBC cells, including screen-printing pastes, and physical vapour deposition (PVD) metal and Cu plating with a suitable barrier layer. In the IBC process development at imec, upscaling from small-area 2cm × 2cm cells to full-area 15.6cm × 15.6cm cells was carried out. In the first instance the 3µm-thick sputtered Al metallization scheme from the 2cm × 2cm cells was adopted. This resulted in cell efficiencies of up to 21.3%, limited by a fill factor (FF) of 77.4%. Besides the limited conductivity of this metallization, the sputtering of a thick Al layer is not straightforward from an industrial perspective; moreover, an Al cell metallization cannot be easily interconnected during module fabrication. A Cu-plating metallization for the large-area IBC cells was therefore investigated, and the scheme is described in detail in this paper. A suitable thin sputtered seed layer for the plating process was studied and developed; this layer serves as a barrier against Cu and has good contact properties to both n^+ and p^+ Si. The sputtering of the various materials could cause damage to the underlying passivation layer and to the Si at the cell level, leading to a lower open-circuit voltage (V_{oc}) and pseudo fill factor (pFF). Reduction of this damage has made it possible to obtain IBC cells with efficiencies of up to 21.9%, measured over the full wafer area of 239cm².

Introduction

Large-area interdigitated back contact (IBC) cells with efficiencies approaching the practical limits of silicon solar cells have recently been demonstrated [1]. The highest reported efficiencies for IBC cells are 25% on a 121cm² area by SunPower, 25.6% on 143.7cm² by Panasonic, and 22.9% on 239cm² by Trina Solar [1–3]. The high efficiencies achieved can be attributed to several advantages of IBC cells, including a fully passivated front surface because of the absence of a front-shading metal grid, and a reduced series resistance because of the possibility of using thick, wide metal contacts on the rear side. However, the metallization of highly efficient cells needs to fulfil certain requirements, such as a low contact resistance to both n^+- and p^+-doped regions, good rear internal reflection, limited influence on the passivation of the doped regions, compatibility with module incorporation, and cost effectiveness. Several metallization schemes have been reported for IBC cells, including screen-printing pastes, and PVD metal and Cu plating with a suitable barrier layer. A review of these techniques, with a focus on Cu plating metallization, is given below.

Fire-through screen-printing process

One of the simplest metallization techniques that has been used for IBC is conventional screen-printing and fire-through of metal pastes [4,5]; it offers advantages such as not requiring dielectric patterning before metallization. However, the firing of the paste can lead to a large contact area between the metal and the silicon, resulting in limited open-circuit voltages because of high contact recombination losses at the contacts. Maximum open-circuit voltages of only 654mV and efficiencies of up to 21.5% have been reported on 15.6cm × 15.6cm IBC cells with this metallization scheme [5].

Standard fire-through Al pastes offer low contact resistance on p^+-doped surfaces, but on n^+ surfaces they may lead to shunting after firing because of Al alloying. Non-alloying Al pastes have recently been proposed as a potential solution to the problem for p-type IBC cells [6]; however, they have not yet been demonstrated in practice.

Ag pastes are typically used for contacting n^+-doped surfaces [7], but can lead to a high cost of metallization [6]. Thus, although the fire-through of metal pastes is a simple process, it can also limit the efficiency potential of IBC cells, because of high recombination at the metal–silicon interface; this method is also potentially expensive if Ag paste is used. These are probably the reasons why this process has not yet been commercialized for large-area IBC cells.

PVD aluminium metallization

PVD Al can offer good contact to both p^+- and n^+-doped surfaces. For n^+-doped surfaces, it has been reported that the specific contact resistance (ρ_c) for Al on n-type Si is very sensitive to the surface concentration of the doping [8]. The value of ρ_c could change from $10^{-3}\Omega{\cdot}cm^2$ to less than $10^{-4}\Omega{\cdot}cm^2$ for a change in surface concentration from $10^{19}/cm^3$ to $2{\times}10^{19}/cm^3$. Thus, as long as the doping concentration at the n^+ surface is greater than $2{\times}10^{19}/cm^3$, Al-PVD-based metallization could be used to contact both p^+- and n^+-type surfaces [9]. Al with a small content of silicon (generally <2%) is used for contacting the p^+ surface [10] in order to avoid shunting of the junction because of Al spiking upon annealing.

A large-area high-efficiency IBC

solar cell process which utilizes AlSi-PVD metallization has been developed at imec. Confirmed efficiencies of up to 23.1% for small-area 4cm^2 cells on 15.6cm × 15.6cm wafers have been demonstrated using photolithography [11]. A best cell efficiency of 22.7% for 4cm^2 cells has been achieved with a photolitho-free IBC process using cost-effective and industrially feasible patterning steps, and a sputtered metallization of 2µm-thick Al [9]. The cell area was then scaled up to an IBC cell of 239cm^2 covering the entire 15.6cm × 15.6cm wafer; the cell design for these large-area IBC cells incorporates several rectangular unit cells connected in parallel [12]. This has resulted in a best cell efficiency of 21.3% [13], limited by a fill factor value of 77.4% for cells with 3µm-thick aluminium, mainly because of high series resistance.

Increasing the fill factor could be partly solved by increasing the metal thickness [4]. Large-area IBC cells (15.6cm × 15.6cm) with a fill factor of up to 78.5% using PVD metallization have been reported by ISFH/Bosch [14], possibly with a much higher Al thickness. In the authors' opinion, increasing the metal thickness by sputtering could lead to increased bowing and also breakage of wafers.

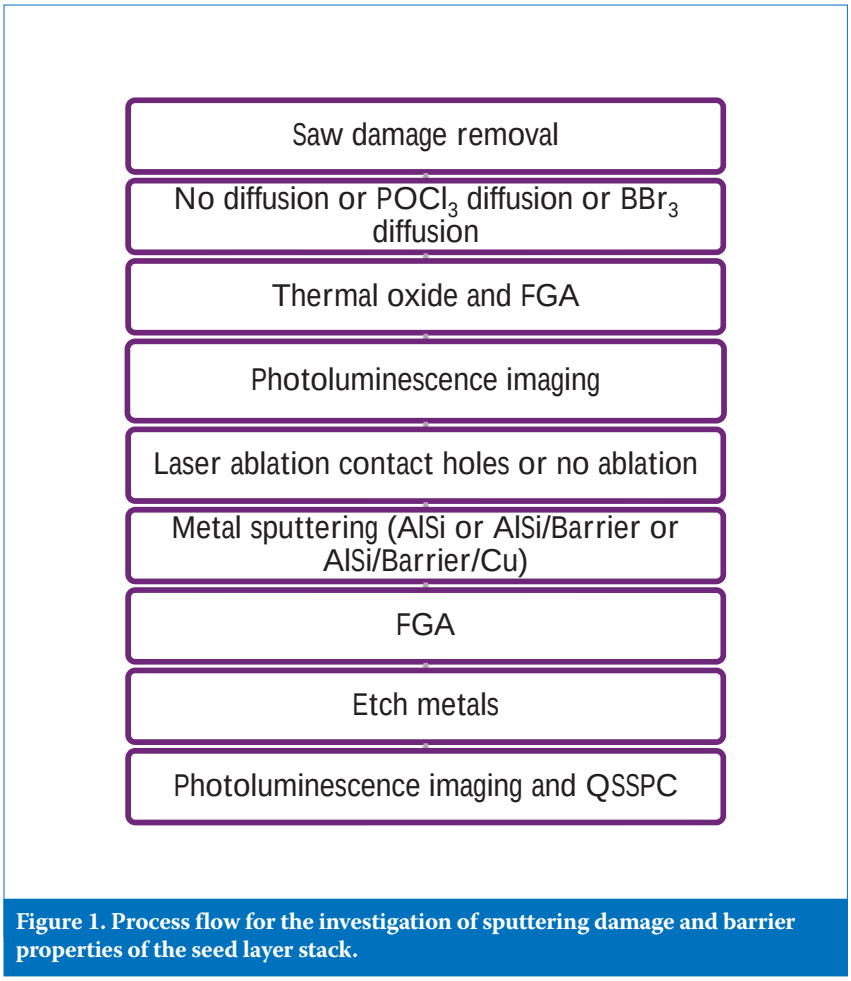

Figure 1. Process flow for the investigation of sputtering damage and barrier properties of the seed layer stack.

Additionally, the sputtering of thick AlSi is neither commercially viable nor readily compatible with cell interconnection [15]. There is therefore a need for an alternative, commercially feasible and module-integration-compatible, thick metal stack for large-area IBC cells.

"Increasing the metal thickness by sputtering could lead to increased bowing and also breakage of wafers."

Cu-plating-based metallization

A seed and Cu-plating process can tackle the challenges mentioned above. Cu-plating-based metallization has been successfully industrialized by SunPower for large-area IBC cells, with best efficiencies of 24.5% for 12.5cm × 12.5cm cells. A Cu-plating process requires a suitable seed layer stack that satisfies the following requirements:

- Good ohmic contact to both p^+- and n^+-doped silicon regions
- High rear-surface reflection
- A barrier for Cu diffusion into the Si
- A suitable layer on top to enable subsequent plating

This thin stack could be easily deposited by sputtering because of the various advantages of the method, such as uniformity, maintaining stoichiometry and conformity [16]. This PVD stack can be less than 500nm thick, clearly less than when a metallization with only PVD is envisaged. A thicker Cu layer can be plated on top of the seed layer.

The sputtering of metal layers, however, has been reported to cause damage to the underlying passivation layer and silicon substrate as a result of bombardment of the surface by photons in the soft X-ray regime [17–19]. For sputtered AlSi layers this damage can be effectively recovered by forming gas annealing (FGA); however, in some cases (e.g. sputtering of metals such as NiV and NiCr), it has been shown that the damage cannot be fully recovered, even after FGA [19].

The results of a study of a seed layer stack for Cu plating and its barrier properties, as well as a detailed investigation of sputtering damage and its recovery by FGA, are presented in this paper. This

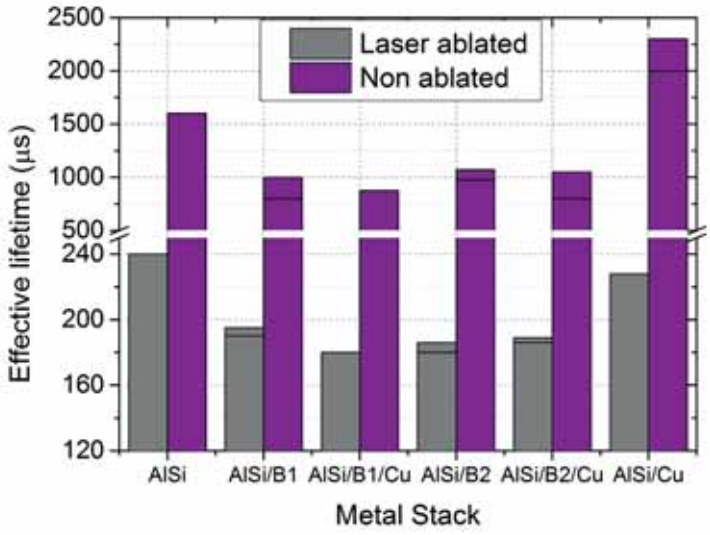

Figure 2. Effective lifetimes (at an injection level of 1E15cm^{-3}) of wafers following the full process flow listed in Fig. 1, without the $POCl_3$ or BBr_3 diffusion.

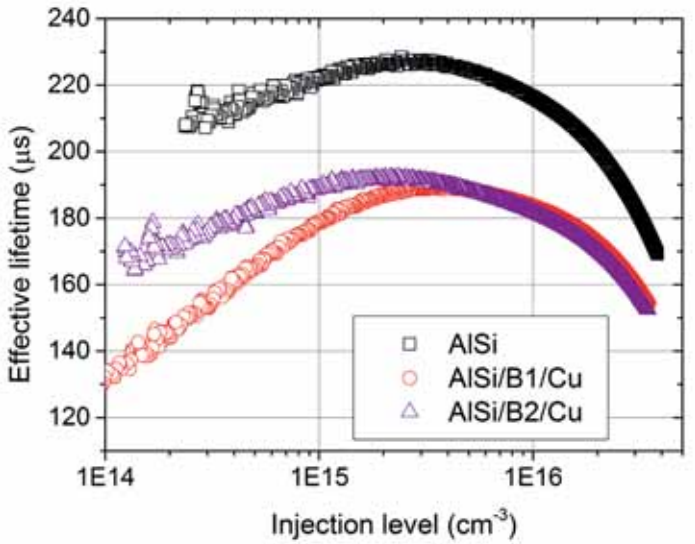

Figure 3. Injection-dependent lifetime of typical samples with different metals stacks.

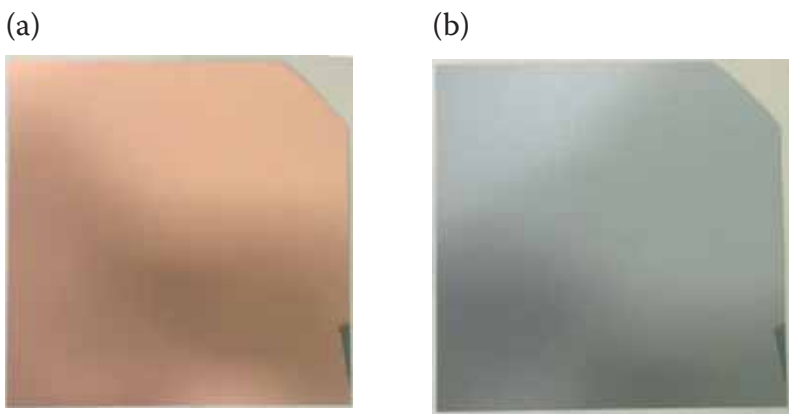

Figure 4. Images of samples with AlSi/Cu: (a) before, and (b) after FGA at 400°C.

seed layer stack and the subsequent Cu-plating process are then integrated in large-area solar cells.

Process flow for sputtering damage investigation

The process flow used for investigating the sputtering damage is illustrated in Fig. 1. Semi-square n-type 15.6mm × 15.6mm CZ silicon wafers first undergo a saw damage removal etch step, then are cleaned, and subsequently either proceed to direct thermal oxidation or undergo emitter (BBr_3) or BSF ($POCl_3$) diffusion. The passivation/dopant activation is carried out by thermal oxidation.

This is followed by FGA and quasi-steady-state photoconductance (QSSPC) measurements. Next, contact areas are defined by laser ablation on part of the wafers, followed by various thin metallization stacks, including two titanium-based barriers, namely B1 and B2. These contact areas also allow the investigation of possible Cu diffusion into the silicon through the barrier. The wafers then receive an FGA, followed by a metal etch and photoluminescence imaging and QSSPC lifetime measurement. In order to analyse the surface defect density *p*, n-type polished and oxidized wafers were used for capacitance voltage (CV) measurements; for these measurements the metallized areas were defined by photolithography after a blanket metal process and subsequent etch of the underlying seed layer.

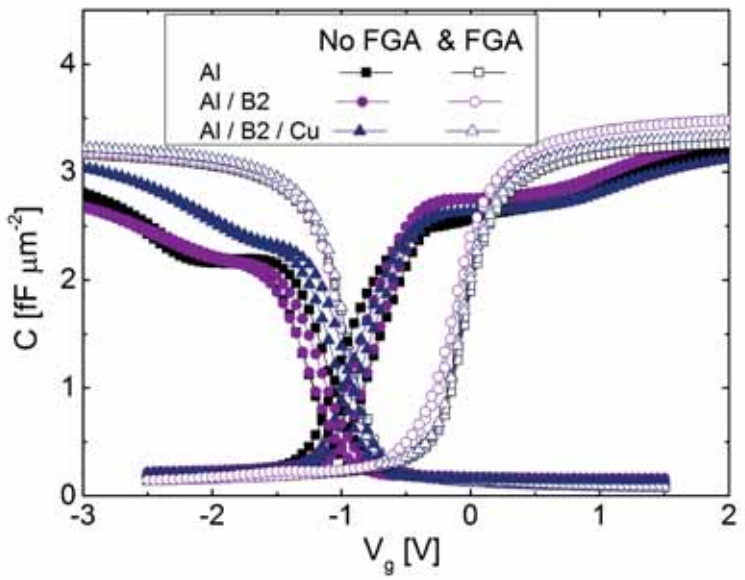

Figure 5. CV measurements for thermally oxidized p- and n-type samples.

Lifetime and CV studies of wafers without BBr_3 or $POCl_3$ diffusion

It is observed from Fig. 2 that samples having undergone laser ablation

demonstrate significantly lower lifetimes than samples without ablated surfaces; this is because there is clearly no passivation present in the laser openings. It is also seen that samples with AlSi/B1 (and B2) display lower lifetimes (≤1ms) than those with only AlSi (>1.5ms), which indicates higher sputtering damage on samples with either of the barriers. It may be noted that in the process flow described above, the metal stack is etched only after FGA in order to retain the benefits from the well-known Alneal effect upon sintering [20]. This is in contrast to the process flow listed elsewhere in the literature [19].

Next, the samples with AlSi/B1/Cu and AlSi/B2/Cu display similar lifetimes as respective samples (AlSi/B1 or B2) without Cu, indicating that the Cu deposition and the FGA at 400°C do not lead to Cu diffusion through the barrier layers, or that such a Cu diffusion has no further negative effect on the lifetime. AlSi/B1/Cu, however, exhibits lower lifetimes in the low injection regime than AlSi/B2/Cu, as seen in Fig. 3.

Barrier B2 was therefore chosen for further investigations on samples with emitter/BSF diffusion. Surprisingly, non-ablated samples with AlSi/Cu demonstrate higher lifetimes (≥2ms) than corresponding samples with AlSi only. This shows that Cu does not cause any significant sputtering damage and possibly results in enhancing the lifetime by an effect similar to the 'alneal' effect [20]. However, this does not imply that no barrier layer would be required, as the laser-ablated AlSi/Cu samples display lower lifetimes than samples with only AlSi, which could be a sign of Cu diffusion in the laser-ablated regions. Furthermore, the discoloration seen in Fig. 4 is visual evidence that Cu could diffuse into AlSi. Various phases of Cu and Al are possible after sintering at 400°C [21], emphasizing the need of a barrier layer to prevent the diffusion of Cu. This discoloration is not observed in the samples with AlSi/barrier/Cu.

Capacitance–voltage profiling (CV) measurements carried out on p- and n-type polished and thermally oxidized silicon wafers are shown in Fig 5. Immediately after the seed layer sputtering step, a large shoulder is present in the CV curves in the region between accumulation and depletion for both n-Si and p-Si substrates. This is consistent with the presence of high densities of silicon dangling-bond defects at the Si/SiO_2 interface, at energy levels between the valence band edge and the mid-gap (p-Si), and from the mid-gap to the conduction

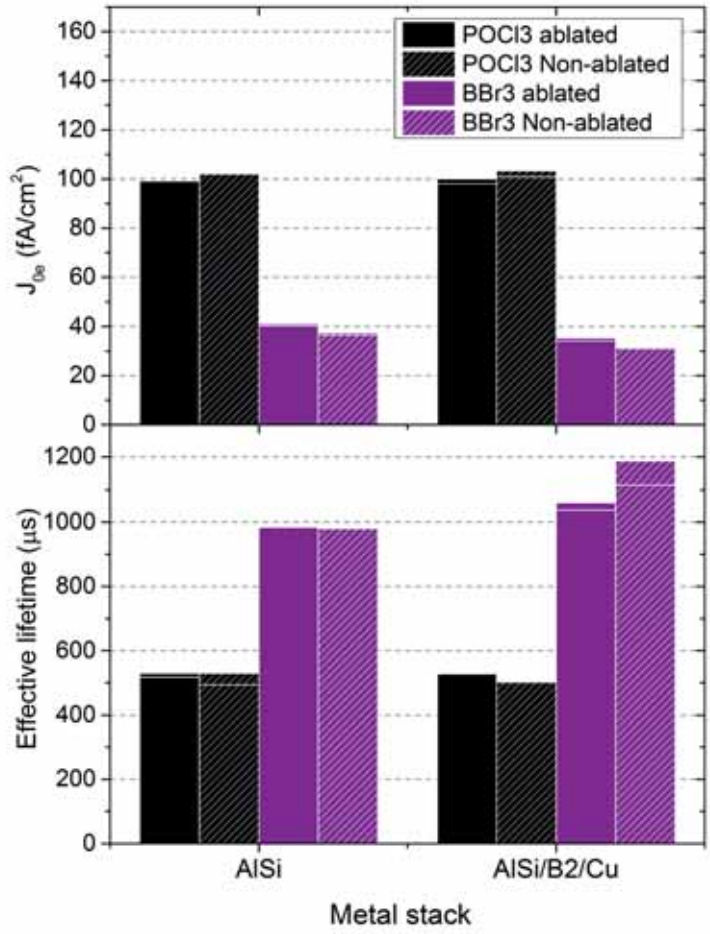

Figure 6. Effective lifetime and J_{0e} for BBr_3-diffused (emitter) and $POCl_3$-diffused (BSF) samples.

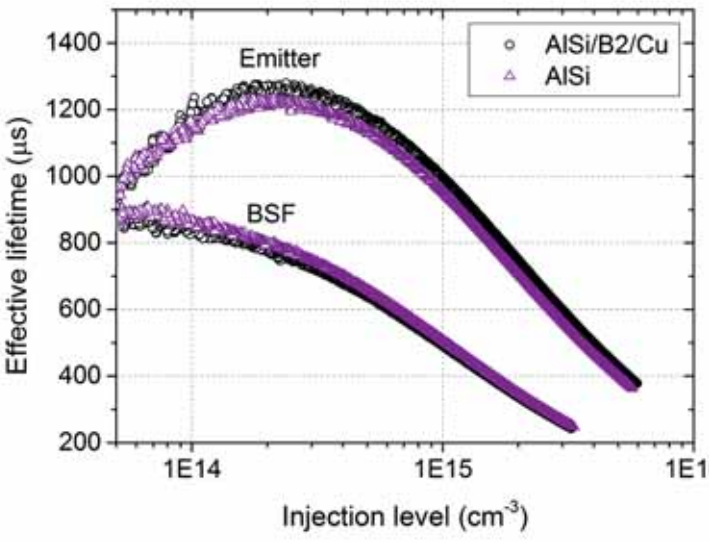

Figure 7. QSSPC curves for BBr_3-diffused (emitter) and $POCl_3$-diffused (BSF) samples.

band minimum (n-Si). These features are removed by FGA, indicating the successful passivation of the interface defects. Negligible hysteresis indicates low densities of trap/defects in the SiO_2 layer after FGA for all samples with AlSi, AlSi/B2 and AlSi/B2/Cu.

> "The differences in effective lifetimes of samples with and without a barrier layer are not related to any remaining surface damage but could be related to the shallow damage below the Si/SiO_2 interface."

It has been reported [22] that sputtering introduces damage near the interface, and that these defects move deeper into the substrate at temperatures above 275°C. These defects were shown to be present up to a depth of 0.5µm. This results in the important conclusion that the differences in effective lifetimes of samples with and without a barrier layer are not related to any remaining surface damage but could be related to the shallow damage below the Si/SiO_2 interface.

Lifetimes studies of wafers with BBr_3 or $POCl_3$ diffusion

In order to understand the effect of sputtering damage on the open-circuit voltage V_{oc} and pseudo fill factor pFF of IBC cells, samples with symmetrical emitter (BBr_3) and BSF ($POCl_3$) doping were prepared. The samples were sputtered with AlSi, AlSi/B2 and AlSi/B2/Cu layers. Lifetime and emitter saturation current (J_{0e}) values measured on these samples with AlSi and AlSi/B2/Cu after FGA (and metal etch) are shown in Fig. 6.

First, it is observed that there is only a very small difference in lifetimes between laser-ablated and non-ablated samples for these diffused wafers (contrary to the case of samples without and with doping, shown in Fig. 2). This can be attributed to the field-effect passivation from the diffused regions masking the surface passivation damage caused by laser ablation.

Second, for BSF-diffused samples, no measurable difference in lifetime or J_{0e} is observed between AlSi and AlSi/B2/Cu. Although the samples with emitter diffusion show slightly better lifetimes for those with AlSi/B2/Cu than the corresponding ones with AlSi, it was found that this is related to the difference between the effective lifetimes of the wafers measured before metal sputtering rather than to the sputtered layers themselves.

These results are also in contrast to the results shown in Fig. 2 for non-diffused samples. QSSPC measurements at low injection (see Fig. 7) do not show any significant difference in effective lifetimes at all injection levels down to less than 5E13/cm^3. It was concluded from these studies (as well as from CV measurements) that additional sputtering damage caused by the barrier layer below the surface is possibly situated in the (highly) doped region of emitter and BSF diffusion. This is also supported by the fact that for the samples with emitter diffusion (shallower doping), the lifetime at low injection levels decreases, whereas for samples with BSF diffusion (deeper doping), it does not.

It is noted that BSF doping profiles are much deeper than emitter doping profiles and extend more than 1µm in depth [9], accommodating all the sputter-damaged region. This is also

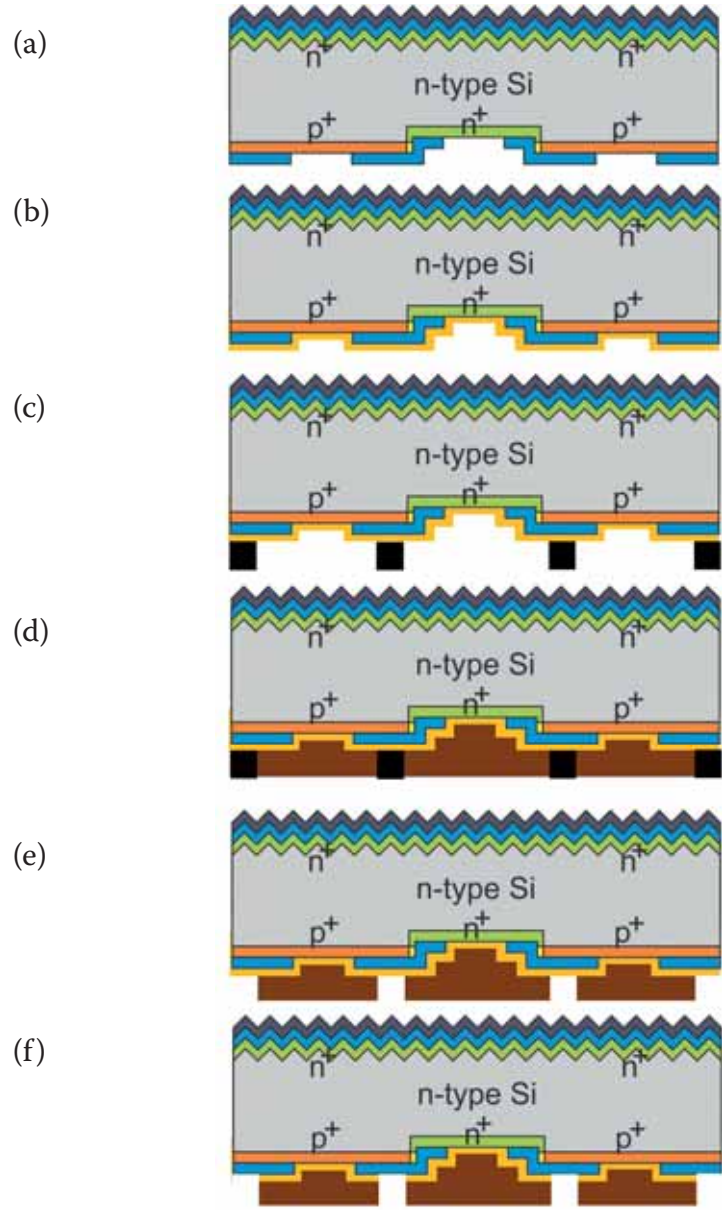

Figure 8. IBC cell metallization flow.

Metal	Size [cm^2]	J_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	Eta [%]	pFF [%]
Cu-plating	239.1	40.64	682	79.0	21.9	83.0
AlSi-PVD	239.1	40.80	686	77.1	21.6	83.6

Table 1. Best *I–V* results for 239cm^2-area IBC cells with Cu-plating and AlSi-PVD metallization.

in line with the above-mentioned fact that the doped regions could screen the surface defects. Therefore, even if this sputtering damage is present, it does not affect the measured effective lifetime and J_{0e}.

Cu-plating process implementation for IBC cells

The chosen seed layer stack AlSi/B2/Cu has been implemented in the IBC cell process – the process flow is depicted in Fig. 8. The previously developed process [9,13] is followed until the opening of the contact areas by laser ablation (Fig. 8(a)). Metallization is carried out by PVD AlSi/B2/Cu blanket deposition (Fig. 8(b)). Emitter and BSF metallized regions are defined by screen printing a resist (Fig. 8(c)), followed by the plating of more than 5µm Cu on the non-masked regions (Fig. 8(d)). Next, a resist strip (Fig. 8(e)) and metal seed etch (Fig. 8(f)) are performed. During the metal seed etch, plated Cu acts as a mask, so the seed layer is only etched in the regions without Cu, which are the regions where the resist was printed. FGA is then carried out, after which *I–V* measurements are taken; Table 1 lists the cell results obtained.

As expected from the lower line resistance of the Cu metallization, cells with Cu-plating metallization displayed a higher fill factor than with 3µm AlSi-PVD metallization. Although the J_{sc} values were similar in both cases, the measured values of V_{oc} were slightly lower in the case of Cu-plated cells; this is being investigated further.

Very high pseudo fill factors were observed for Cu-plated samples, indicating the absence of shunts in metallization; this confirms that the developed seed layer (barrier) is effective against Cu diffusion and substantiates the potential for such a metallization scheme. Finally, an efficiency of 21.9% measured over the full area of 239.1cm^2 cells was achieved with Cu-plated IBC cells.

Conclusions

A review of different metallization schemes for IBC cells – such as screen-printed pastes, PVD metal and plated Cu with a seed layer – has been presented. The firing-through of screen-printed metal pastes is a simple process, but it can limit the efficiency potential of IBC cells, because of the high recombination at the metal–silicon interface; moreover, it can be expensive because of the use of Ag paste. In the authors' view, PVD metallization – such as the sputtering of thick AlSi – is neither commercially viable nor readily compatible with cell interconnection.

> "The developed seed layer and Cu plating process has been integrated for large-area IBC cells, resulting in cell efficiencies of up to 21.9% on the full area of the cells."

Owing to its various advantages, a thin seed layer followed by Cu plating was therefore chosen and investigated in detail. This metallization stack satisfies the various requirements of high-efficiency large-area industrial IBC solar cells; these requirements include low contact resistance to both n^+- and p^+-doped regions, limited influence on the passivation of the doped regions, good compatibility with module incorporation, and cost effectiveness. The developed seed layer and Cu plating process has been integrated for large-area IBC cells, resulting in cell efficiencies of up to 21.9% on the full area of the cells. To the best of the authors' knowledge, this is the highest efficiency measured for IBC cells of 15.6cm × 15.6cm with Cu-plating metallization.

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